MULTISYSTEM TEST EQUIPMENT

UNITED STATES ARMY MISSILE COMMAND

AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION

RCA

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Contract DA-36-034-ORD-3650 Z

MULTISYSTEM TEST EQUIPMENT

Prepared for:

COMMANDING GENERAL
ARMY MISSILE COMMAND
REDSTONE ARSENAL, ALABAMA
ATTN: AMSMI-RHD

Prepared by:

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BURLINGTON, MASSACHUSETTS

FOREWORD

Radio Corporation of America submits the Multisystem Test Equipment Fourth Quarterly Interim Technical Report, in response to the requirements of paragraph 7.3 of TR 160 Revision No. 3, dated 29 January 1962.

This report is submitted to Army Missile Command Redstone Arsenal, Alabama under Contract DA-36-034-ORD-3650 Z.

This quarterly report covers the period from 1 January 1963 to 31 March 1963.

REPORT APPROVAL

This Fourth Quarterly Interim Technical Report has been reviewed and approved by:

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SECTION I

INTRODUCTION

Factory production commenced during this quarter on standard printed circuits for the computer in the Electronic Test Set.

Factory production of other MTE system hardware is starting. During this quarter, 18 standard types of millimodules and 16 standard types of millimodule boards were designed and released for production. These will have wide application as MTE building-blocks and are designed to perform satisfactorily under "worst case" conditions of maximum parts tolerances and degradation of transistor current gain due to temperature or end-of-life conditions.

Other items are being readied for release to production. Drawings were completed for the rack and chassis mechanical configurations. The rack detail drawings will be completed when the environmental design tests, started this quarter, have been completed. A shelter-rack interface has been developed. Final modifications will be made when shock and vibration tests, started this quarter, have been completed.

Extensive detailed design work is continuing on the Electronic Test Set equipment. The logical design and performance specifications for the computer are nearly complete. The logical design of the controller is approximately 70% complete. Vendors have been recommended for all items of peripheral equipment. Layouts have been finalized and circuits are being designed for the display/control equipment. Extensive design, breadboarding, and testing work has been accomplished on all of the other units comprising the Electronic Test Groups. Preliminary work on software for the computer has commenced.

On 24 January 1963 RCA subcontracted to Greer Hydraulics Inc., Los Angeles, California, the design, development, fabrication, and test of the Hydraulic and Pneumatic Test Stands for the Hydraulic Test Set. During this quarter the subcontractor has done approximately half the study work required to establish the system design of the Stands.

Estimates of the reliability of the Electronic Test Set and the Hydraulic Test Set indicate that present designs are approaching the reliability goals. Work on a maintainability prediction for these Test Sets has been started.

The design of the entire MTE system is under constant review. The relative merits of two independent Electronic Test Sets as compared with the present design is reported herein. A draft of a report on the Repair Support Set has been published separately. Further documentation on Mauler and other missile systems was received and analyzed. This has permitted more definitive design work on this Contract Support Sets. Moreover, testing of the Lance missile system can be accomplished under present MTE concepts, according to preliminary information.

Other work of overall significance in the performance of the MTE system has been accomplished. The MTE test plan has been further developed. The requirements of TR-160 can be met by the design concept of self-test and fault isolation developed this quarter. A single-point grounding system has been designed for MTE.

For improved transportability, the weight of Electronic Test Group No. 1, Electronic Test Group No. 2, and the Hydraulic Test Group has been reduced 941 lb, altogether. The cooling and ventilating of the equipment racks was studied thoroughly this quarter.

SECTION 2

STUDIES AND PRESENTATIONS

2.1 TEST REQUIREMENTS ANALYSIS (TRA)

2.1.1 OBJECTIVE

To establish for Army missile systems appropriate testing procedures and programming requirements.

2.1.2 PROGRESS

A broad scope of work was carried on during the quarter toward the objective. The several areas of effort consisted of (1) establishing testing procedures and programming requirements, (2) establishing testing requirements, (3) acquisition of documentation on missile systems, and (4) a study of Mauler UUTs to typify the advantages that will accrue if two independent Electronic Test Sets are approved (see Section 3.2).

Testing procedures and programming requirements are being prepared for the Mauler UUTs listed in Table 2-1, for which testing requirements have been previously established.

Mauler radars test requirements have been established according to a complete set of schematics on the engineering model. The data was received and analyzed during this quarter and confirmed much of the preliminary work previously done. In addition, testing requirements have been established for the Mauler Launch Order Computer and Fire Control Unit. The documentation for this work was also received and analyzed during this quarter. This determination of testing requirements has permitted the establishment of requirements for the waveform analyzer adaptor for measurement of pulse width, use time, amplitude, and other characteristics. The documentation on the Launch Order Computer provided data on the mechanical configuration of this unit and some of its subassemblies and

data on connector locations, which will be of value in establishing whether the UUTs are to be tested inside or outside the shelter and the cabling requirements.

The Lance Missile System was broadly described by Ling - Temco - Vought personnel during a visit to their plant in Dallas, Texas. The information is preliminary due to the early stage of the Lance program. However, all testing requirements presented are within the scope of present MTE concepts.

Quantity of missile system documentation received during the quarter is listed in Table 2-2. Percentage of required documentation received to date is tabulated in Table 2-3. No documentation on Shillelagh was received during the quarter. Documentation requested from Army Missile Command during the quarter is as follows:

RCA Letter Number	Date	Missile System
ECR: MTE: 177	11 February	Pershing
ECR: MTE: 184	15 February	Mauler
ECR: MTE: 186	25 February	Task and Skill Analysis References
ECR: MTE: 194	5 March	Pershing

Mauler subassemblies were re-evaluated to establish the units that could be tested by each of the MTE Electronic Test Sets if an independent test set configuration is authorized. This configuration would provide microwave stimuli and liquid cooling in Electronic Test Set No. 2. Therefore, the UUTs to be tested by these Electronic Test Sets were separated into (1) those requiring microwave stimuli <u>or</u> liquid cooling and (2) all others. A tabulation of typical UUTs requiring microwave stimuli <u>or</u> liquid cooling is given below.

Acquisition Radar	Track Illumination Radar
Isolator - (coolant)	Klystron Oscillator - μwave and coolant
Switch Tube - (coolant)	Heat Sink Circulator - μwave and coolant
Stabilotron - (μwave and coolant)	Body and Dummy Load - μwave and coolant
HV Power Supply - (coolant)	Klystron Amplifier Collector - μwave and coolant
LV Power Supply - (coolant)	Local Oscillator Power Supply - coolant
Stabilizing Cavity - (μwave and coolant)	HV Power Supply - coolant
	LV Power Supply - coolant

Table 2-1. Priority testings of Mauler UUTs

PRIORITY I	PRIORITY II	PRIORITY III
1. Round (less warhead and motor) (410-010030)	1. Missile Sequencer (LOC) (410-074001)	1. TEC Memory Output Assy (5A1) (10096701)
2. Receiver Main IF Unit (Acq.) (10091073)	2. Servo Assembly (LOC) (410-072001)	2. TEC Flux Lok Memory assy (5A2) (10097000)
3. Electric Synchronizer (Acq.) (10090042)	3. Receiver First Detector (Acq.) (10091431)	3. TEC Memory Input Assy No. 1 (5A13) (10097104)
4. Speedgate (TI-9A1) (10091402)	4. Data Converter (Acq.) (10090959)	4. TEC Memory Input Assy No. 2 (5A9) (10094103)
5. Azimuth Servo Hydraulic Valve (1076914)	5. Stalo Coho Assy. (Acq.) (10092154)	5. TEC Arithmetic Unit Assy No. 1 (5A4) (10096704)
6. TEC Input/output Assy. No. 1 (5A8) (10096708)	6. Synchrodyne Driver (TI) (10091381)	6. Active Display Assy (WCC) (410-060240)
		7. FSK and Intercom (DTCU) (666082-352)
		8. Missile Scanner Assy (LOC) (410-073001)
		9. Speedgate (TI-9A2) (10091420)

Table 2-2. TRA Documentation received during Quarter

	Mauler	Shillelagh	Lance	AAD570	Nike Zeus	Sergeant	Pershing	Hawk	Nike-Hercules	Lacrosse
1. Schematics	170						1	23	44	
2. Test Proc.	14									
3. Assy Dwgs										
4. Wir. Diag										
5. Des. Cont. Dwg										
6. Tm's	61						2		2	1
7. Sys. Desc.										
8 Rmoc's					8					
9. Spec's	9						3	10		
10. Gen. bk dwn								36		

Table 2-3. Percentage of Documentation Received

	Mauler	Shillelagh	Lance	AAD570	Nike Zeus	Sergeant	Pershing	Hawk	Nike-Hercules	Lacrosse
1. Schematics	60	30	0	0	10	25	85	90	85	95
2. Test Proc.	10	0	0	0	10	50	40	25	35	90
3. Assy Dwgs	25	80	0	0	10	80	50	5	5	90
4. Wir. Diag	1	0	0	0	0	1	20	20	30	80
5. Des. Cont. Dwg	95	0	0	0	0	1	0	60	60	85
6. Tm's	95	50	0	0	15	80	95	90	90	95
7. Sys. Desc.	95	80	25	0	50	90	95	100	100	100
8. Rmoc's	30	0	0	0	25	10	0	80	75	80
9. Spec's	30	0	0	0	0	50	45	30	40	95
10. Gen. bk dwn	60	50	0	0	95	10	80	100	100	100

2.1.3 TRA PLANS

Additional testing procedures and programming requirements will be established during the next quarter. This effort will be concentrated on five Mauler UUTs listed under Priority I in Table 2-1 and the five UUTs from other missile systems listed in Table 2-4. As additional documentation is received, testing requirements will be continually updated.

Table 2-4. Missile systems UUTs

Missile System	G. S. or Ord. Number	UUT Title
Nike Hercules	17747	±320 volt Power Supply
Nike Hercules	153846	DC Amplifier
Nike Hercules	17622	Elect. Cont. Amplifier
Nike Hercules	58678	Interval Timer
Hawk	10043328	Antenna Control

2.2 CONTACT SUPPORT SET STUDY

2.2.1 GENERAL

Contact Support Set effort consists of a Battalion Contact Support Set Study and a parallel Missile Contact Support Set Study.

2.2.2 BATTALION CONTACT SUPPORT SET STUDY

A. Objective

To define the configuration, capability, and employment of a Battalion Contact Support Set (BCSS) to provide contact team support. The BCSS has the immediate goal of supporting the Mauler weapon pod but with sufficient capability to extend support to the AADS-70, Lance, Shillelagh and Tow missile systems with minimal modification.

B. Progress and Status

Initial effort on this task has resulted in a somewhat complex equipment configuration to perform the BCSS task. This came about because of two factors:

(a) the lack of detailed Mauler and other missile system information at that time dictated a conservative approach to ensure applicability to a number of future missile systems;

(b) only standard MTE modules were used to minimize development.

Accordingly, the current study effort is directed toward reducing the complexity of the BCSS to the equivalent of four standard MTE racks.

Discussions with experienced field maintenance personnel indicates the need for a rapid cable-checking facility in the BCSS. It is expected that the manual test equipment available at 2nd echelon plus the self-test features built into the Mauler weapon pod will enable fault isolation to a major assembly by the 2nd echelon maintenance team. Therefore, the BCSS will be required to isolate faults that may be caused by cabling failures in addition to combinations of assembly failures and limitations or failures of the self-test system.

C. Plans

It is planned to complete the BCSS study during the next reporting period. To accomplish this, a number of trips will be made to obtain system test requirements to supplement data received in the form of schematics, specifications, and maintenance manuals. Continued liaison will be necessary with cognizant AMICOM agencies to ensure that the study properly reflects Army maintenance philosophy and needs.

2.2.3 MISSILE CONTACT SUPPORT SET STUDY

A. Objective

To define the capability, configuration, and employment of a Missile Contact Support Set (MCSS) that will provide a high degree of confidence in the operational readiness of missile rounds before issue to forward area missile batteries and firing units by the ammunition supply points.

The MCSS concept is based on the need for rapid pre-issue and verification testing of missile rounds by Ammunition Supply Points (ASP) or Special Ammunition Supply Poin' (SASP). Due to the high flow rates associated with this type of testing, an automatic go-no-go test capability is required to permit high volume testing by relatively unskilled personnel. The MCSS should also provide the capability of isolating missile malfunctions to replaceable sections which could then be routed to the MTE complex for higher echelon maintenance.

B. Progress

A preliminary study of MCSS requirements and equipment feasibility has been completed. From this study a basic concept for the MCSS has evolved which provides for rapid screening of missile rounds.

C. Design Concept

The logical method to attain the objective is to simulate pre-launch and in-flight conditions to the maximum extent possible while monitoring missile performance. This requires dynamic input-output tests to assure satisfactory missile performance.

In addition to this dynamic type of testing requirement, a fault isolation test mode is required; this can be achieved by a go-no-go type of testing where several outputs would be monitored serially to permit logical selection of the faulty section.

2.3 REPAIR SUPPORT SET STUDY

2.3.1 OBJECTIVE

To determine the requirements for supplementary repair and support facilities in platoons and detachments equipped with Multi-System Test Equipment and to recommend configurations to meet the requirements. An additional objective was to determine the feasibility of combining the functions of the Contact Support Set and the Repair Set.

2.3.2 STATUS

The study has been completed, requirements have been established, and equipment has been recommended to satisfy the requirements. A report has been written and is presently in the process of publication.

One unfinished aspect of the study concerns the questionnaire sent to overseas missile field installations to obtain data in addition to that obtained domestically. Should an analysis of this overseas data modify the conclusions of the study, this will be discussed in a future Quarterly Report.

2.3.3 CONCLUSIONS

A. General

Items of standard issue - shelters, tools, test equipment - have been found applicable to the requirements for MTE Supplementary repair and support functions. Certain of these items of standard issue will require modification, but no new shop set designs are required. All sets recommended could be supplied GFE and modified where necessary.

B. Repair Support

The study recommends that MTE repair support be implemented along functional lines through an Electronic Repair Group and a Mechanical Repair Group, composed respectively of a modified Pershing Electrical Repair Support Set and Mechanical Repair Support Set.

The basic equipment complement of these Pershing Sets would be kept intact except for the deletion of Pershing-peculiar equipment and the addition of that special equipment required by the Missile System(s) to be supported.

The principal modifications concern equipment layout in the shelters and are detailed in the study report.

C. Supply and Management Support

The study recommends that: the supply support functions be provided through the use of a modified Pershing Supply Management Set, a modified Pershing Supply Support Set (storage) Type I, and a modified Pershing Supply Support Set (storage) Type II; the preservation and packaging function be provided through the use of a modified Pershing Preservation and Packaging Set; and the shop operation control and communications function be provided through the use of a modified Pershing Supply Management Set. The required modifications are relatively minor.

D. Combined Missile Support and Repair Set

Combining of the functions of the Contact Support Set with those of the Repair Set has been determined not feasible. The reasons for separation of these functions are:

(1) The tool and equipment requirements of the two functions differ to a great degree. The Contact Support Set Function has extensive test equipment requirements for system test capability and less comprehensive tool requirements than has the Repair Set Function.
(2) It is not tactically desirable to delete the repair capability of the MTE platoon by detaching the Repair Set facilities for Contact Support missions.
(3) The mobility requirements are not compatible. The Contact Team must be capable of fast response regardless of terrain; adding the tool and equipment requirements of repair support to the vehicle used for Contact Support would decrease this fast response capability.

(4) The parts complements differ for the two functions. The Repair Support function requires storage of a large number of small repair parts whereas the Contact Support Function requires a capability for selection of appropriate replacement items from the Direct Exchange (DX) supply as required by a specific mission call.

2.4 TEST PLAN FORMULATION

2.4.1 OBJECTIVE

To establish a composite plan for all tests to be performed on deliverable equipment through final acceptance tests. Tests will be performed at all levels of assembly starting at the printed circuit board level.

2.4.2 PROGRESS

The MTE Test Plan, described in the MTE Third Quarterly Interim Technical Report CR-63-547-31 and shown in Figure 2-1 of that report, was developed as a generalized flow-type plan for the test and integration of the MTE system.

This plan has been further developed and detailed, and now consists of eight general levels of tests. A slightly modified version of Figure 2-1 of the Third Quarterly Report is reproduced as Figure 2-1 in this report and has the eight levels of tests superimposed on it. The eight levels of tests are briefly described below while Figure 2-2 designates the responsibility for the documentation and approval required at each level.

1. 1st Level Intra-Unit

   This level of testing encompasses the thorough testing of any one assembly.

2. 2nd Level Intra-Unit

   This level of testing is performed on two or more assemblies that have been through 1st level testing, integrates and tests them. In some instances, the assemblies may form a functional loop.

Considering the Mauler missile as representative of the missiles which will receive pre-issue testing at the ASP, the pre-launch and in-flight inputs to the missile and the missile responses would be accomplished with the round remaining within the integral shipping canister (launch tube) to minimize testing time. To permit fault isolation to a replaceable section, the round must be removed from the canister to expose additional test points.

D. Equipment Concept

The MCSS equipment concept resulting from the study would use, whatever possible, building blocks identical to those in the MTE system, while keeping the size and complexity of the set to a minimum. This approach will result in substantial savings in logistics and maintenance due to the capability of direct substitution with MTE units.

Where new equipment is required, MTE standard circuits and components will be utilized to the maximum possible extent.

The MCSS is envisioned as a self-sustaining operational unit mounted on a standard M-36 or M-55 truck (MTE type air transportable shelter), or on an XM-546 tracked vehicle as required.

E. Plans

The planned outputs from the MCSS study during the next quarter are:

(1) MCSS Configuration (Functional Block Diagram)
(2) Overall MCSS System Specifications
(3) MCSS Subsystem (Unit) Specifications
(4) Suggested MCSS Employment
(5) Specifications for Special Tools and Equipment.

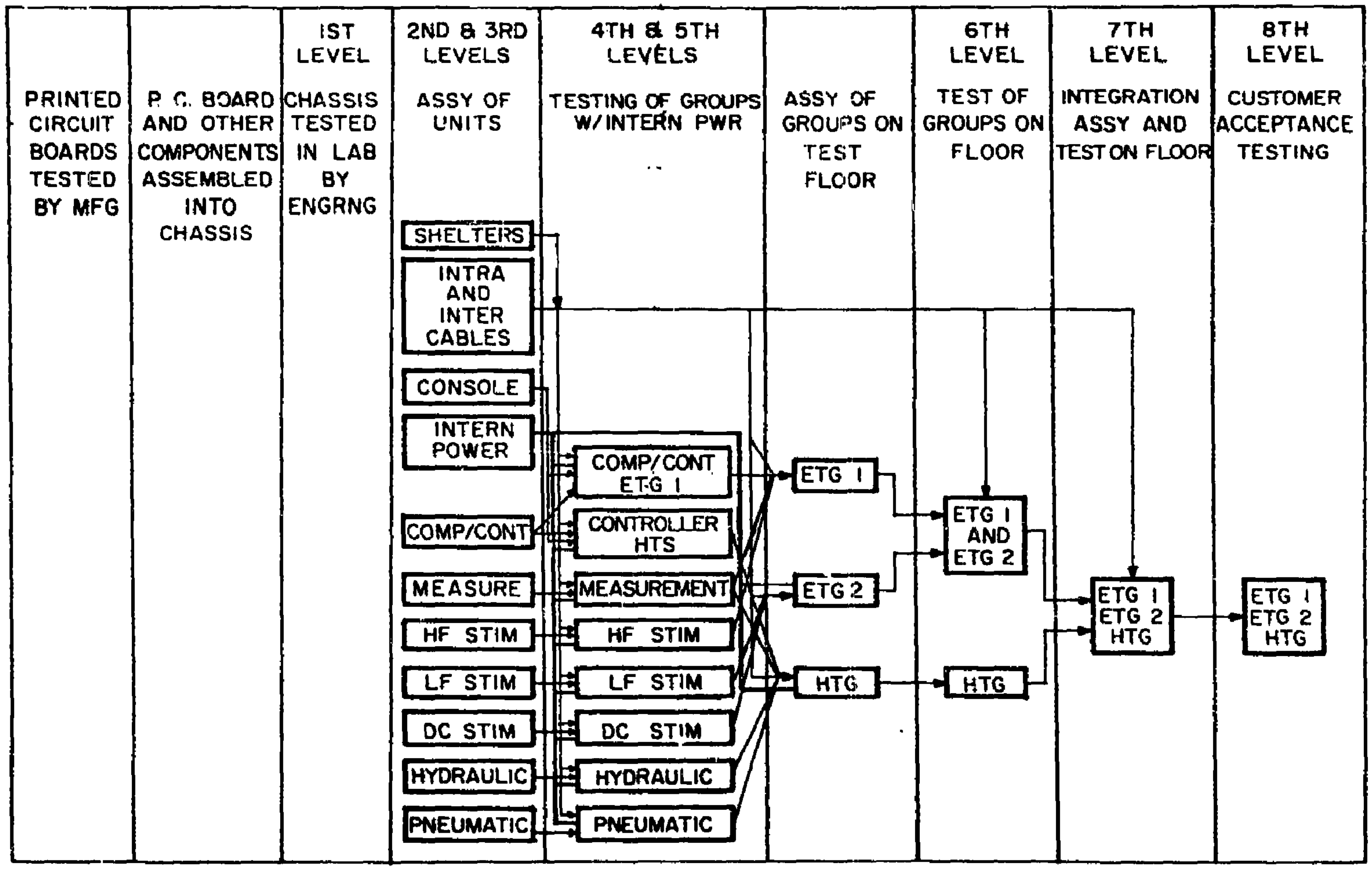

Figure 2-1. Generalized MTE test plan.

Activity \ Tests	Millimods, Boards, Sub-assy	1st Level	2nd Level	3rd Level	4th Level	5th Level	6th Level	7th & 8th Level
Test Activity	Mfg.	Des. Engr.	Des. Engr.	Des. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.
Test Area	Factory	Engr. Lab.	Engr. Lab.	Engr. Lab.	Integ. Floor & Shelters	Shelters	Shelters	Shelters
Test Specifications								
Prepared by	Des. Engr.	Des. Engr.	Des. Engr.	Des. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.
Approved by	P.A.	Sys. Engr. P.A.	Sys. Engr. P.A.	Sys. Engr. P.A.	P.A.	P.A.	P.A. Des. Engr.	P.A. AMC
Test Procedures	Mfg.	Des. Engr.	Des. Engr.	Des. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.	Sys. Engr.

Figure 2-2. Test activity responsibility.

3. 3rd Level Intra-Unit

   This level occurs when all the functional loops of one specific unit are integrated to comprise the entire unit. This level will include EMI & RFI testing.

4. 4th Level Inter-Unit

   This level of testing is the integration and test phase of the Computer/Controller, Measurements and Internal Power Supplies for both the ETS & HTS. Completion of this level provides a central operating establishment for the balance of the integration and test program.

5. 5th Level Inter-Unit

   This phase of testing introduces the stimuli units individual to the overall system for integration and test.

6. 6th Level Inter-Set Tests

   This level occurs when any two or more sets have been completely tested and are integrated and tested as a system.

7. 7th Level MTE Self-Test

   This level occurs when the entire MTE has been integrated and can perform as a complete Test Equipment establishment. All self-test modes will be exercised during this phase.

8. 8th Level Acceptance Test

   This level of testing occurs after the entire system has been submitted to the 7th level test phase, installed in the shelters and re-run through levels 6 & 7. The system is presented to the customer at this level.

Individual test and integration plans have been prepared by each design group. Figure 2-3 is an example of the plan prepared by the systems engineering group for the Computer/Controller. Each circle and oval represents a test and/or integration step for which a test specification and test procedure will be written. Each of the group plans is then combined into a systems integration plan (Figure 2-4).

2.4.3 PLANS

Plans for the next quarter are as follows:

(a) A preliminary Acceptance Test Plan will be generated and will be submitted to AMICOM.

(b) Cognizant design groups will start the generation of test specifications for 1st, 2nd, and 3rd level tests.

(c) A Draft of the System Test & Integration Plan will be started.

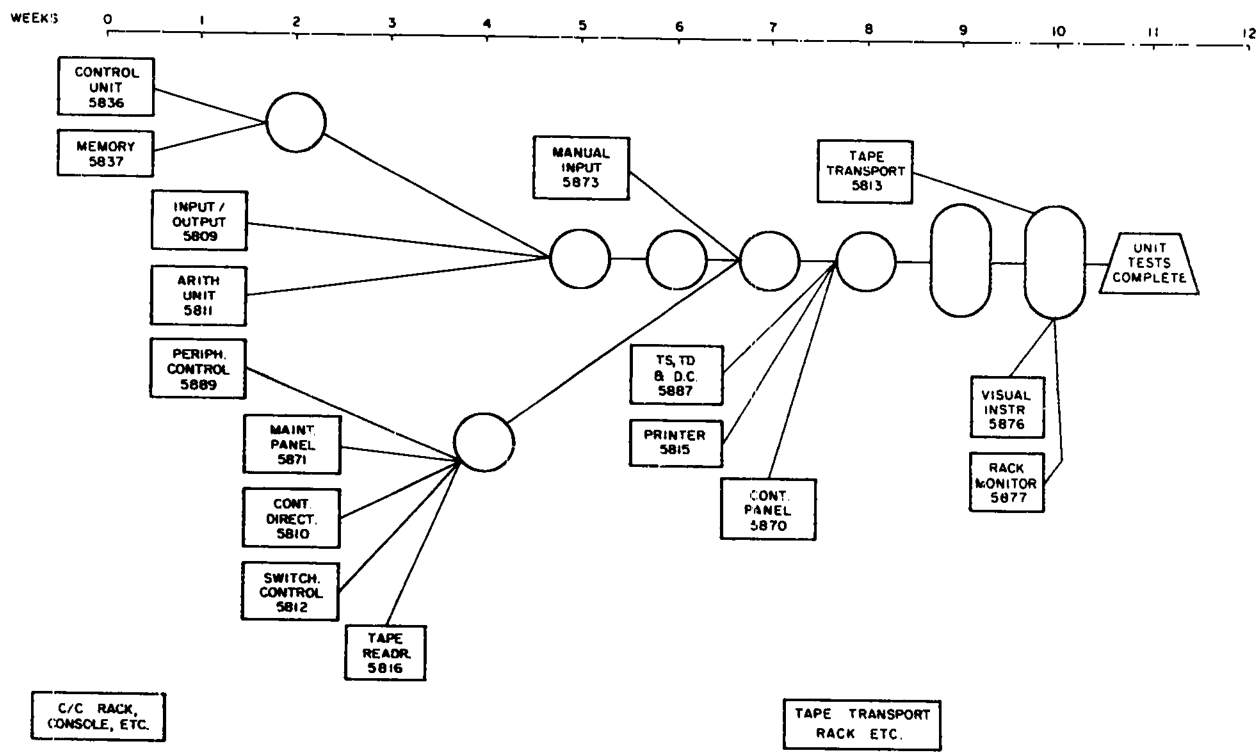

Figure 2-3. Integration and test plan - computer/controller.

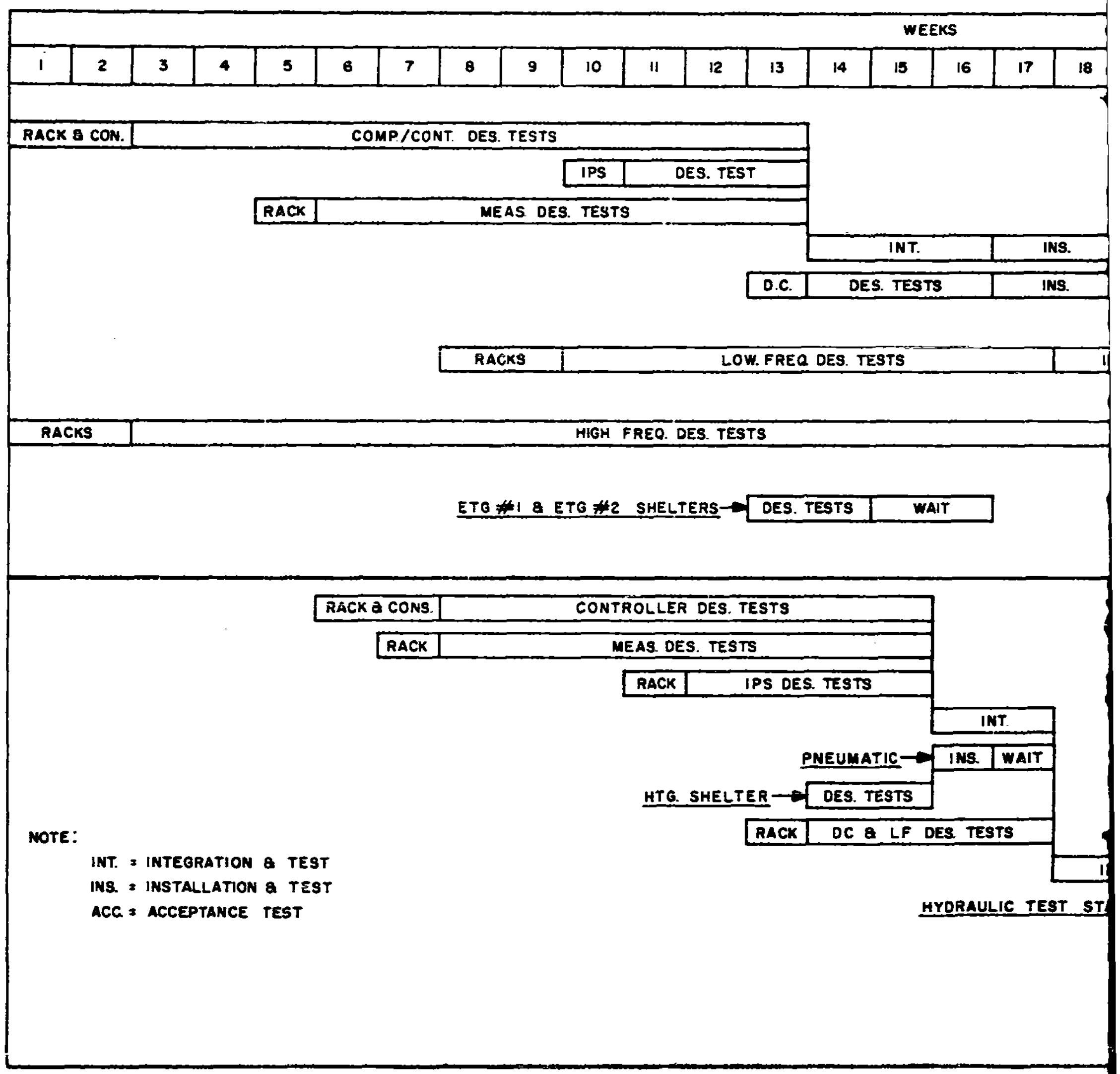

Figure 2-4. Integration and test plan -

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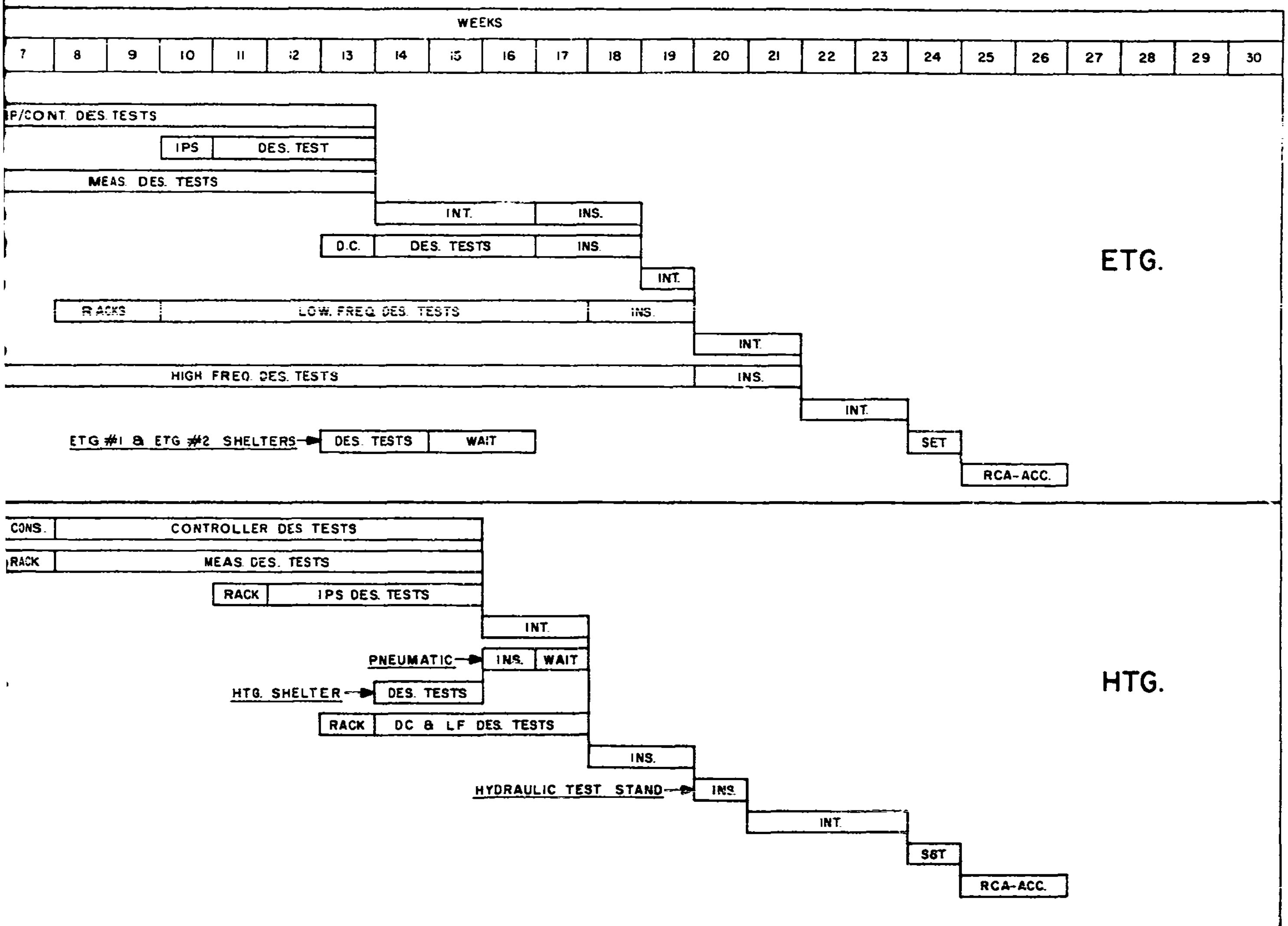


Figure 2-4. Integration and test plan - ETG, HTG.

SECTION 3

SYSTEM DESIGN

3.1 INTRODUCTION

MTE System capability is under continual review against technical and operational requirements as system design and development progresses. A major item of system review during this quarter consisted of an investigation of an MTE configuration of two independent Electronic Test Sets. This effort is reported in Section 3.2 below

System Specifications are also under continual review. Approximately 25 changes have been made to MTE specifications during this period; these will be delivered to AMICOM for review and approval through normal channels. Section 3.3 outlines the more important of these modifications.

The Self-Test and Fault Isolation techniques used in the MTE System are outlined in Section 3.4; while Section 3.5 discusses System Grounding Techniques.

3.2 INDEPENDENT MTE ELECTRONIC UNIT CONFIGURATION

3.2.1 INTRODUCTION

During the MTE Design Configuration Review held at RCA during February 1963, it was suggested by Army Missile Command personnel that RCA investigate an MTE Configuration of two independent Electronic Test Sets that would offer improved efficiency and increased flexibility. This report submits the results of this effort.

3.2.2 PRESENT MTE CONFIGURATION

The present MTE configuration consists of an Electronic Test Set with equipment housed in two shelters, and a Hydraulic Test Set in one shelter The two shelters housing the Electronic Test Set (ETS) are

interconnected at all times and operate as an integrated unit. The Hydraulic Test Set (HTS) operates either independently of the Electronic Test Set or under control of the Electronic Test Set.

With this configuration, Mauler electronic UUT's are tested one at a time; the average test times for such UUT's is given in the MTE TRA report dated 6 December 1962.

3.2.3 NEW CONFIGURATION

A. Concept

The new configuration, discussed below, achieves the objectives of increased efficiency and flexibility by designing two Electronic Test Sets, one in each shelter, and capable of two modes of operation: (1) independent operation, and (2) operation wherein ETS No. 1 controls the ETS No. 2 or the HTS.

B. Description

Electronic Test Set No. 1 will have the capability of performing low frequency and DC testing while Electronic Test Set No. 2 will have the capability of performing high frequency (microwave) and DC testing plus the capability of testing those UUTs requiring the Liquid Cooler.

The major items comprising ETS No. 1 are (see Figure 3-1).

(1) Operator's Control Console
(2) Computer/Controller
(3) Measurements
(4) Low Frequency Stimulus
(5) DC Stimulus
(6) Internal Power Supplies
(7) Power Distribution and one 45-kw Generator
(8) 3 Air Conditioners

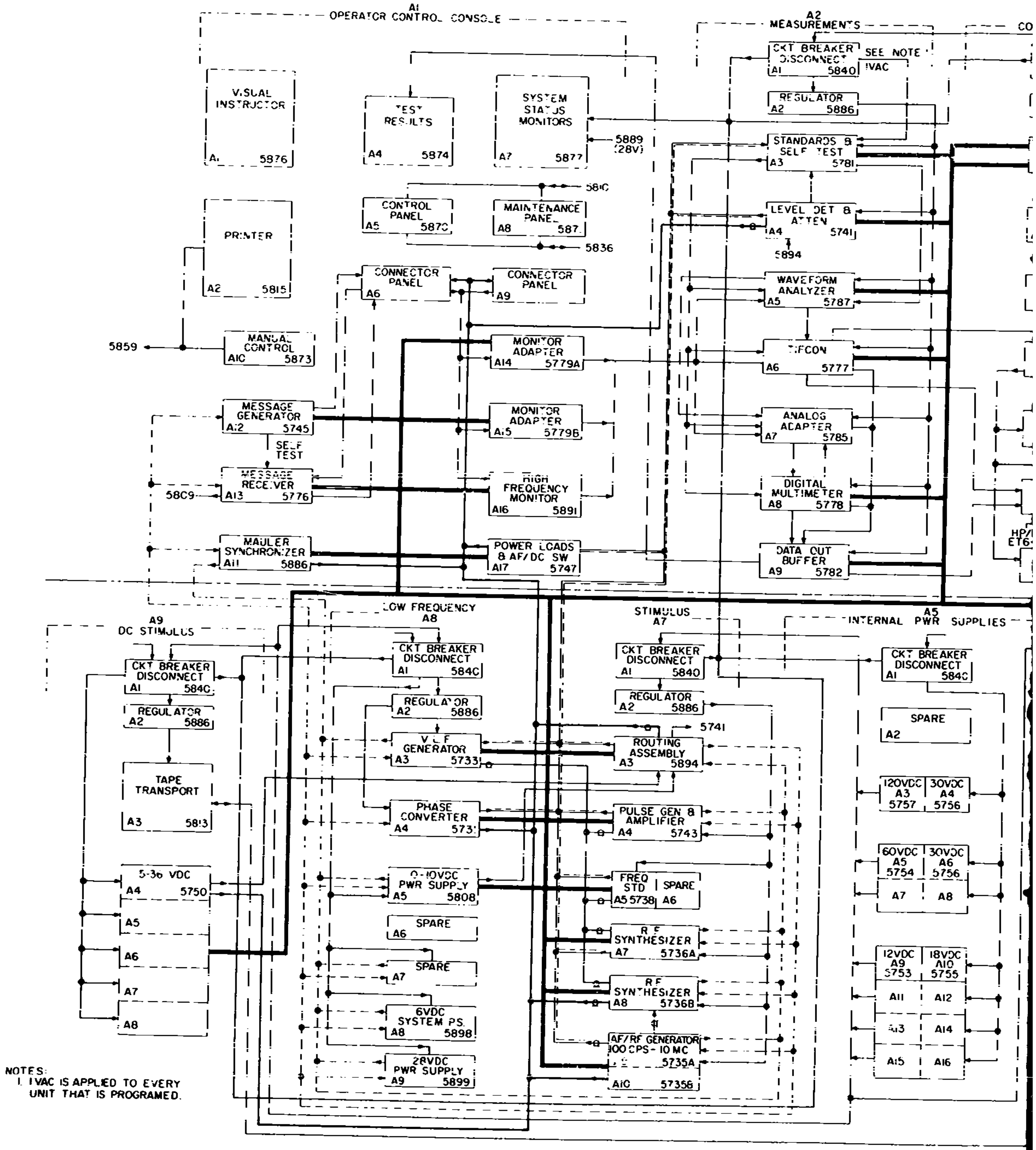
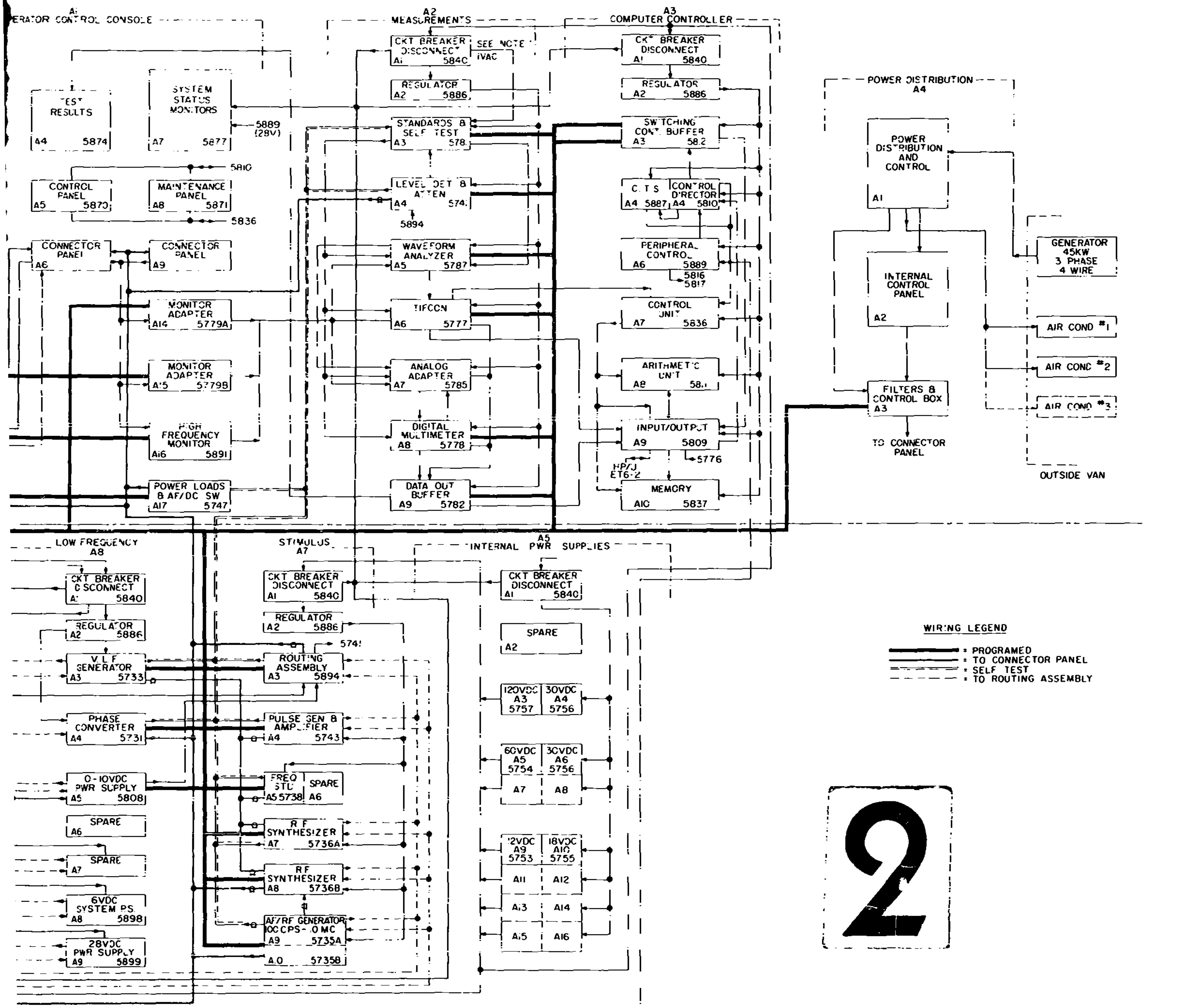


Figure 3-1. Electronic Test Set No. 1 - block diagram.



Electronic Test Set No. 1 - block diagram.

The major items comprising ETS No. 2 are (see Figure 3-2).

(1) Operator's Control Console
(2) Controller
(3) Measurements
(4) Partial Low Frequency Stimulus
(5) High Frequency Stimulus
(6) DC Stimulus
(7) Internal Power Supplies
(8) Power Distribution and one 45-kw Generator
(9) 3 Air Conditioners
(10) UUT Cooler

It should be noted that the basic difference between the two sets is the use of a Computer/Controller in ETS No. 1 contrasted with the use of a controller only in ETS No. 2. In addition, it should be noted that the Operator's Controller Console and Measurements equipment are the same for the two sets although a magnetic tape transport will be used with the Computer/Controller of set No. 1 while a tape reader will be used in conjunction with the controller in set No. 2.

The DC stimulus groups of the two sets are similar although set No. 2 has two additional DC stimuli namely, 250-850VDC and 20-300 VDC. These are required because Microwave UUTs require higher DC voltage stimuli than the low frequency UUTs of the Mauler system.

The low frequency stimulus capability of the two sets differ because ETS No. 1 requires the availability of a complete range of low frequency stimuli while ETS No. 2 only requires the following assemblies from the low frequency equipment unit in order to perform microwave UUT testing:

(1) Frequency Standard
(2) Pulse Generator and Power Amplifier
(3) AF/RF Generator

(4) Message Receiver

(5) Low Frequency Routing Assembly

The Internal Power Supplies of the two Electronic Test Sets differ because the voltage and current requirements for the testing done by the two sets are different.

C. Additional Components

The additional chassis required by the new configuration (including the Circuit Breaker Disconnect Chassis and Regulator Chassis) total 45.

D. Mechanical Configuration

Since the two Electronic Test Sets in the new configuration have indentical Operator Control Consoles and Measurement Units; the left side wall of each is identical except for the Computer/Controller rack. In ETS No. 2 the Controller rack will house the Low Frequency Stimulus Unit. Thus, with the exception mentioned above, the left side wall of the new configuration is identical to the present configuration.

In the new configuration the right side wall of the two Electronic Test Sets will also be similar; containing the DC Stimulus, Internal Power Supplies, and Storage, plus different Low Frequency and High Frequency Stimulus racks.

E. Equipment Weight and Power Consumption

The tabulations below summarize the weight and power consumption of each ETS in the new configuration.

(1) Weight - ETS No. 1

(1)	MTE Equipment	2487 lbs
(2)	Shelter plus two air conditioners	2321 lbs
(3)	Racks and Cables	2244 lbs
(4)	Junction Box	60 lbs
(5)	Additional Air Conditioner	300 lbs
	Total	7412 lbs

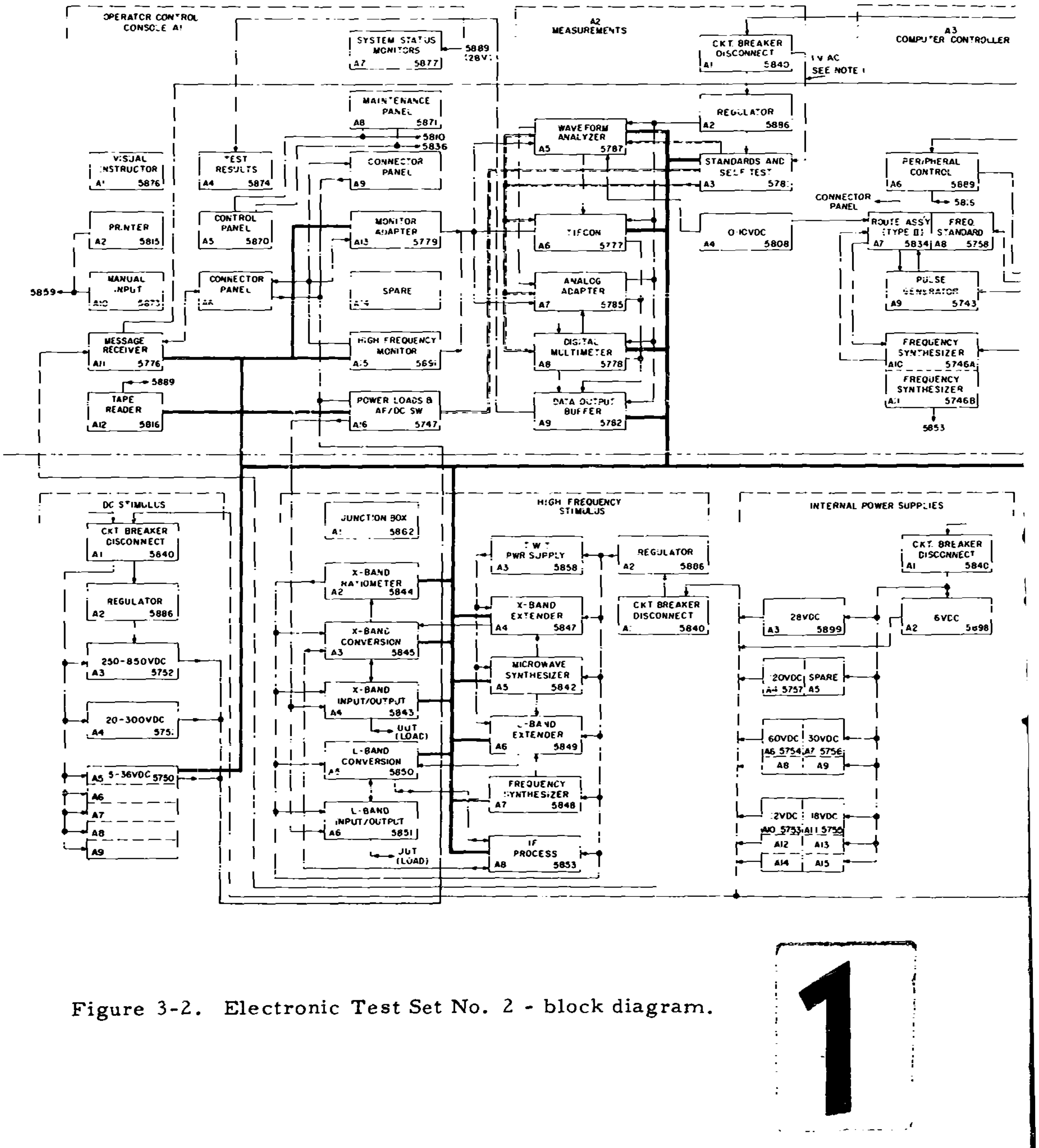
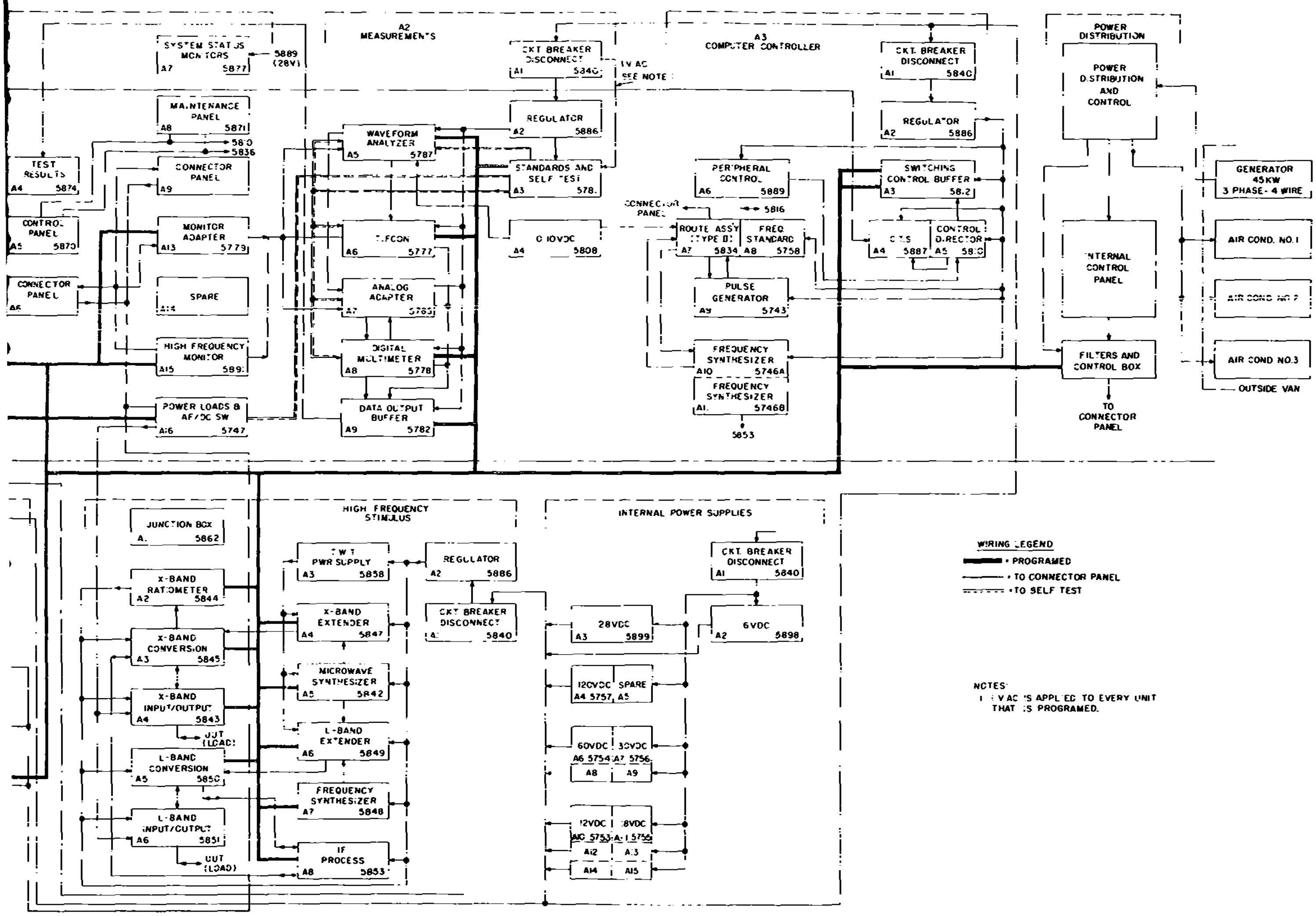


Figure 3-2. Electronic Test Set No. 2 - block diagram.

1



Electronic Test Set No. 2 - block diagram.

2

(2) Weight ETS No. 2

(1) MTE Equipment		2476 lbs
(2) Shelter plus two air conditioners		2321 lbs
(3) Racks and Cables		2244 lbs
(4) Junction Box		60 lbs
(5) Cooler		150 lbs
(6) Additional Air Conditioner		300 lbs
	Total	7551 lbs

(3) Power Consumption ETS No. 1

(1) Internal MTE Equipment dissipation		10, 750 watts
(2) Shelter (including two air conditioners)		14, 100 watts
(3) Additional Air Conditioner		6, 600 watts
(4) UUT Use		5, 000 watts
	Total	36, 450 watts

(4) Power Consumption ETS No. 2

(1) Internal MTE Equipment dissipation		10, 176 watts
(2) Shelter (including two air conditioners)		14, 100 watts
(3) Cooler		350 watts
(4) Additional Air Conditioner		6, 600 watts
(5) Maximum UUT Load (1 case only)		11, 000 watts
	Total	42, 226 watts

3.2.4 SUMMARY

A. <u>Number of Test Stations</u>

It is apparent that with the present configuration a maximum of two test stations is available (one in ETS No. 1 and No. 2 combined and one in the HTS). The new configuration has three test stations, an increase of 50% in overall testing capability and a potential increase of 100% in electronic testing capability.

B. Improved MTE Utilization

The availability of two electronic test stations, one in each Electronic Test Set, each capable of independent testing will allow low frequency and power supply UUTs to be tested at one station (ETS No. 1) and Microwave and power supply UUTs to be tested at the second station (ETS No. 2).

Three advantages accrue from this mode of operation:

(1) The degree of utilization of MTE equipment is radically increased.
(2) The rate of UUT processing is nearly doubled (not quite double because ETS No. 2 with its Controller operates slightly more slowly than does ETS No. 1 with its Computer/Controller)(Note: Set up time is usually more than test times.)
(3) The separation of Microwave test equipment from the low frequency equipment. Since some missile systems do not require microwave capability, only the appropriate Electronic Test Set need be used. Conversely, two ETS No. 1 units can be used to double the rate of low frequency testing capability.

A very important advantage, in addition, is the ability to add additional high frequency or low frequency capability by adding only one hut to an existing set-up.

C. Rate of UUT Testing

From page 6-44 Table 6-9 of MTE TRA report dated 6 December 1962, the average test time for an electronic UUT is 29.4 minutes (including processing time, disposition time, connection time, etc.). The processing time is given as 3.8 minutes and the disposition time as 3.7 minutes, totalling 7.5 minutes or approximately 25% of the 29.4 minutes average test time.

With the two electronic test stations in the new configuration, the processing and disposition times might increase slightly since UUTs are being routed to and from two test stations rather than one. It is unlikely that the processing and disposition time of 7.5 minutes would increase more than 1/3.

An additional factor influencing the UUT handling rate is the fact that the Electronic Test Set No. 2 will handle UUTs slightly more slowly than Electronic Test Set No. 1 since ETS No. 1 has a computer/controller while ETS No. 2 has only a controller.

The overall time added to the 29.4 minutes to account for the above should be 7.5 minutes or less to handle two UUTs instead of one, resulting in an increase of at least 75% in the rate of UUT handling or resulting in a corresponding decrease in the time to test a given volume of UUTs.

D. Reduced Cabling Between Shelters

The independent operating capability of the two Electronic Test Sets in the new configuration results in a reduction of inter-shelter cabling as follows:

(1) Wires and coaxial cables carrying low frequency stimulus signals, pulse generator signals, pulse power outputs and signals to attenuators and levelers are eliminated along with the concomittant drivers and pulse shapers.
(2) All power cabling between the two Electronic Test Sets is eliminated.
(3) Fewer control lines are required between sets.

As an estimate, 200 wires and 21 coaxial cables presently running between the two electronic groups are eliminated in the new configuration.

E. Mean Time Between Failures

The Mean Time Between Failures (MTBF) for the present configuration has been estimated at 40 hours. The estimated MTBF for the new configuration is 78 hours for ETS No. 1 and 52 hours for ETS No. 2.

F. Increased Number of Chassis

The independent ETS configuration contains approximately 45 additional chassis over the present configuration. No new chassis designs are required.

G. Increased Cabling Within Each Set

An estimated 15% increase in cabling complexity within each independent Electronic Test Set results from the additional chassis of the new configuration.

H. Test and Integration

ETS No. 1 and No. 2 can be integrated in parallel, simplifying the integration process.

I. Additional Air Conditioners

Each shelter needs one additional air conditioner to handle the increased heat load.

J. Added Weight

Each shelter of the new configuration increases in weight to between 7000 and 8000 lbs.

K. Effect On Schedule

Due to the 45 additional chassis required in the new configuration, equipment releases must be changed to provide the additional material. Bulk material and long lead items required for the present configuration have been ordered over the past 2 1/2 months. This time is lost re-ordering additional items and will cause an estimated one month delay in completion of ETS No. 1 and No. 2 to the new configuration.

L. Working Spares

The identical chassis of the two Electronic Test Sets provide a source of working spares in the event of unit failure.

M. Programming

The programming for the testing of high frequency UUT on ETS No. 2 will be more complex than would be the programming for similar UUTs, were a Computer/Controller available.

3.3 SPECIFICATION ADDITIONS AND/OR MODIFICATIONS

3.3.1 WAVEFORM ANALYSIS

TRA-derived test requirements show the need of waveform analysis capability in the MTE System. This capability will be included in the system and the next quarterly report will describe the functional use and capability of the waveform analyzer.

3.2.2 INTERNAL POWER SUPPLIES

A. Package Size

The size of each internal power supply package has been reduced by 50%, to a half-level chassis instead of a full-level chassis for each. Two factors made this size reduction possible:

(1) A change in the specification of power supply input line voltage regulation. The input line regulation was originally specified as +10% and -15%. Since the MTE GFE generators are specified to 1% voltage tolerance, the power supply specifications have been changed to call for the specified output regulation with this 1% input line regulation over the zero to full-load range. This permits line voltage regulation equipment to be eliminated.

(2) Increased Packaging efficiency.

B. Programmable Power Supply Ranges

Because of the difficulty of furnishing the maximum required current at low voltage from one programmable regulated power supply, the range to be covered has been split into two parts to be covered by two programmable supplies:

(1) 3-15VDC in 0.1 volt steps at 10 Amps max.

(2) 5-36VDC in 1.0 volt steps at 15 Amps max.

Three 3-15VDC supplies and two 5-36VDC supplies are required in place of five 0-36VDC supplies.

3.3.3 CONSOLES

During this reporting period on consoles in ETG-1 and HTS were re-laid out to make them structurally identical. There will, however, be different electrical assemblies in each of them

3.3.4 EQUIPMENT ADDITIONS

A Low Frequency Stimulus Routing Assembly (MTE 5894) and a Mauler Synchronizer Assembly (MTE 5896) have been added to the System. The routing assembly provides flexability in Switching signals within the LF sub-system. The Mauler synchronizer is a Mauler peculiar equipment which generates unique timing pulses. These assemblies are described in Paragraph 6.1.4 of this report.

3.3.5 EQUIPMENT DELETIONS

The Rate Table (MTE 5880) and the Tape Punch (MTE 5817) have been deleted from the system at the request of AMICOM.

3.3.6 EQUIPMENT RELOCATED

The Monitor Adapter (MTE 5869) has been relocated to the pedestal of the Control Console at the request of AMICOM.

The UUT Connector Panel has been moved from the face of the Monitor Adapter to the face of the Control Console at the request of AMICOM.

The Resistive Loads (MTE 5787) and the DC/AF switch (MTE 5747) have been combined into a single assembly located in the space previously occupied by the tape punch assembly.

The Tape Transport (MTE 5813) and the Tape Reader (MTE 5816) are now mounted in the same rack.

3.4 SELF-TEST AND FAULT ISOLATION

3.4.1 GENERAL

An MTE self-test and fault isolation philosophy was established during the past quarter to fulfill the requirements of TR-160.

3.4.2 SYSTEM CONSIDERATIONS

The MTE System will provide programmed self-testing and automatic monitoring self-test.

A. Programmed

This consists of a programmed computer (or in the case of the HTS, a paper tape-controlled self-test which uses the internal standards or inherent signal generation and measurement capability) to check the system. Faults will be isolated to a chassis level within each unit. When tapes are not available or the tape transport is inoperable, manual control of the system is possible; and self-test capability at reduced speed may be achieved by following standard procedures. Programmed tests may be extended to isolate faults within the chassis and subassembly level. Provision will be made to perform UUT-type tests on each MTE chassis. Additional test connectors will be added when necessary to permit fault isolation to a replaceable plug-in functional subassembly. The unit chassis must be removed from its rack to perform these tests; the chassis must be replaced if its function is required in the system for any of the tests.

B. Automatic Monitoring Self-Test

Diagnostic lamps continuously indicate operational status and malfunctions whether or not the particular chassis is being used in a test sequence. Each chassis in MTE includes selected points that are monitored with miniature red "Fault" Keystone Lamps. Outputs from these points are combined and displayed as a single red "Fault" indicator lamp on the rack monitor panel in the Operator's Control Console. The logic voltage for each fault circuit is established as follows:

1. An indicated fault - +6 volts dc
2. An indicated good (or go) - zero volts

Special provisions will be made for rapid isolation of any power malfunction, since these failures are the most serious.

Both digital and analog monitoring are included in the lamp indications. Digital monitoring is limited to visual verification of logic. Functions and instructions displayed on Amperex type 6977 gas tubes which can be directly triggered from logic levels within the computer/controller or peripheral controlled equipments.

Certain parameters in digital areas may be continuously monitored by red "Fault" indicator lamps, these being:

1. Certain repetitive signals
2. Clock pulses
3. Clock sine-wave signals

The fault indicators are implemented by: (1) logic checking circuitry, such as parity and address verification; and (2) signal tracing indicators. In certain cases, voltage comparisons are made to ensure operation within specifications.

The dual self-test capability is particularly important when the computer or controller is inoperative. Automatic monitoring is designed specifically to isolate catastrophic faults and provide the operator with the required information to restore the power system and computer/controller functions to operational status. Programmed tests then provide basic confidence testing for the remainder of the system.

3.4.3 GENERAL SYSTEM PHILOSOPHY - COMPARISON OF SELF-TEST METHODS

The two types of self-test, programmed and automatic monitoring, are capable of accomplishing many of the same functions. As a guide to their use, the following advantages and disadvantages of each type are listed.

A. Programed Self-Test

Advantages

1. No additional equipment required.
2. No increase in equipment cost.
3. No change in overall reliability, since parts count not increased.
4. Can provide complete system confidence check.
5. Once the program is debugged, little maintenance cost is associated with the self-test.
6. Provides the only satisfactory means of dynamically testing complex logic arrays.

Disadvantages

1. Can test only those areas of equipment under program control.
2. Increases the initial programming time and cost.
3. Requires that computer and/or controller and tape systems be operable for Stimuli and Measurement self-test.
4. Requires that complete set of tape programs be available.

B. Automatic Monitoring (Wired-in) Self-Test

Advantages

1. Provides continuous monitoring
2. Can monitor digital registers, pulse chains, voltage levels, power, DC and AC signals to any appropriate accuracy.
3. A powerful inherent fault isolation technique is provided by dynamic checks such as parity for tape and memory, and by verification of proper addressing of MTE subassemblies.
4. Self-test monitor allows programmed system self-test to be run without operator intervention.
5. Additional connections are not required.
6. Can be used when computer and/or controller are inoperative.
7. Particularly valuable in fault isolation of the power system and computer/controller area.
8. Reduces mean time to repair.

Disadvantages

1. Increases cost and complexity of system. Part, count increase results in slight reduction in reliability.
2. Maintenance of self-test portion of system is required.

In the design of the MTE system, these advantages and disadvantages have been considered and the self-test was chosen to produce results consistent with the design objectives previously stated.

3.4.4 PROGRAMMED SELF-TEST

Programmed self-test and fault diagnosis for MTE require the use of taped programs. These programs are written from flow charts which describe the self-test sequence. Test flow charts are converted to computer language and written on magnetic or paper tape for use by operating personnel. To clarify the types of programmed self-tests to be used with MTE, the following are defined.

System Test

A complete MTE self-test program which proves that all MTE unit subsystems are operational and within normal operating limits. This test may be of relatively long duration and used initially in accordance with the Acceptance Test Specification for customer acceptance. This program would be run periodically during normal MTE operation.

Sub-System Test

A program that tests all subsystem elements to be used on a given UUT test. It determines the status of all required subsystem elements in MTE. This test is essentially a small portion of the MTE system test program and may precede a UUT test.

Safety Test

A brief test routine inserted during a UUT test to insure that application of a stimulus will not endanger equipment or personnel by application of incorrect stimulus values to equipment.

Diagnostic Self-Test

A test to isolate the area or element causing a suspected fault. Such programmed tests can be written for the computer internal timing and control, arithmetic assembly, computer memory, and all digital input/output devices and control as well as each stimulus and measuring assembly. Since the use of functional cards has been extended throughout the MTE System, these tests can be utilized in isolating faults to a single card in many cases without the necessity of removing the assembly and treating it as a UUT.

MTE-UUT Test

Typical UUT diagnostic programs written for specific assemblies of the MTE system. In some cases, such as the Analog Adapter, it will be necessary to replace the suspected assembly within the subsystem to run the program. A programmable DC power supply need not be replaced since it is not required as part of the automatic testing equipment.

Basically, all of the above self tests fall into two classes; confidence and diagnostic types. The confidence tests assume that no faults exist and the program fails if a fault is found. Diagnostic tests assume one or more faults. Their function is to isolate the fault to specific hardware components.

3.4.5 AUTOMATIC MONITORING SELF-TEST

Automatic monitoring self-test is accomplished by an integrated network of monitored test points. Each monitored chassis contains fault information on its inputs, outputs and selected internal points which are monitored for failure. Failure in most cases represents an absence of signal which turns on a local red light. Each chassis contains its own malfunction display and a single malfunction output line. These lines are combined to give a single rack or unit malfunction output. The rack malfunctions are then displayed on the Rack Monitor Panel located at a central position in the system.

A. System Monitor and Control Panel

The System Monitor and Control Panels for the Electronic Test Set and the Hydraulic Test Set are located on the Operator's Control Console where the

operator can visually monitor the status of each major subsystem or unit. This panel directs the attention of the operator or the maintenance personnel immediately to the unit causing the system malfunction. The panel displays white and red lamps, oriented according to the physical location of each unit within the Test Set. White indicates normal operation; red indicates malfunction, both lamps off indicates power off. A test button lights all lamps simultaneously for lamp testing. If a fault affects the test in progress or endangers personnel or equipment, an audible alarm sounds. A separate reset switch allows the operator to turn off the alarm for each rack.

B. Circuit Breaker Disconnect Panel

This panel and associated chassis perform the following self-test associated functions: (1) provides means for turning off each power input at the unit rack for maintenance; (2) provide circuit breaker overload protection to the rack; and (3) combine all rack chassis malfunctions with relay logic to provide a single rack malfunction output line.

C. Chassis Monitoring - General

The goal for individual monitoring is to have the light monitoring system detect any catastrophic failure in the chassis. Where possible, the fault should be isolated to a major functional area of the sub-assembly.

In order to detect a fault, the output must be monitored for presence. This is the most basic monitoring point.

Any chassis fault will be displayed by a red lamp indication on the panel. This lamp will indicate that one or more catastrophic failures have been detected. The specific area of the fault will be shown in a small numbered display located on the panel. Provisions have been made for up to twelve such indications in a standard assembly. These lamps are referred to as Keystone Lamps. A single output will be used to indicate a fault for the chassis. A fault will be indicated by +6 volts. No fault (normal operation) will be indicated as zero volts.

D. Circuit Monitoring Requirements

In the light monitoring system a careful choice must be made between those parameters that can be monitored simply and reliably and those that pose expensive and complex problems. Each monitor must provide basic infromation either of inoperability or location of a fault. The requirements of a monitor are that it be more reliable than the equipment that is being monitored, particularly in stability and drift characteristics within specified temperature and environmental conditions.

Two classes of information are monitored in MTE:

1) Digital information in the form of levels used in the digital circuits. This class requires operator knowledge for interpretation. The two levels 0 and +6 allow very simple monitoring of gates and registers (Amperex 6977 indicators).
2) Qualitative information indicating presence or absence of an analog quantity such as DC voltage, RF voltage, or AC power. This monitor always indicates a catastrophic type failure (Keystone Lamp indicators).

The two classes of monitors used in MTE for self-test and fault isolation are described in detail in the following paragraphs.

a. Digital Monitoring

Monitoring of digital circuits for maintenance purposes will be displayed by use of the Amperex 6977 triode. This tube has been used in many RCA military equipments and has an excellent reliability record. The tube is designed for a 20,000 hour life and can be operated directly from logic circuits since only three volts are required to turn the tube off.

Using a 100,000 ohm isolating resistor the loading effects of this tube are negligible on the associated circuit.

These units are used to monitor all programmable registers in stimulus and measurement groups, as well as in the computer and controller.

b. Analog Monitor

The monitoring of the presence (or absence) of an analog quantity, such as DC levels, RF or AC power, is achieved by using standard circuits in conjunction with Keystone Lamp indicators. The basic circuit is the MTE standard milli-module lamp driver. The lamp is turned on when a logical one is applied to any input. In order to reduce the amount of panel space required to display the many monitored points on a chassis, a cluster of Keystone miniature lights are used. These are located on the chassis in a removable bracket.

3.4.6 OPERATIONAL PROCEDURE

During the courses of UUT testing by MTE, certain normal routines are implemented by the use of self-check and fault isolation. Figure 3-3 shows a sample self-test and fault routine.

3.4.7 PLANS FOR NEXT QUARTER

The self-test and fault isolation philosophy discussed in this section is being used in establishing Operational Procedures for MTE. These procedures will be formally submitted with proposed designs for the necessary control, Maintenance and Monitor panels for AMICOM review and approval during the next reporting period.

3.5 MTE GROUNDING SYSTEM

3.5.1 PURPOSE

The purpose of the grounding system is to insure a system free from ground loops so that noise and interference signals will be held to a minimum.

3.5.2 PHILOSOPHY

A single point ground system will be employed, isolating AC primary power return current from the internal signal ground bus.

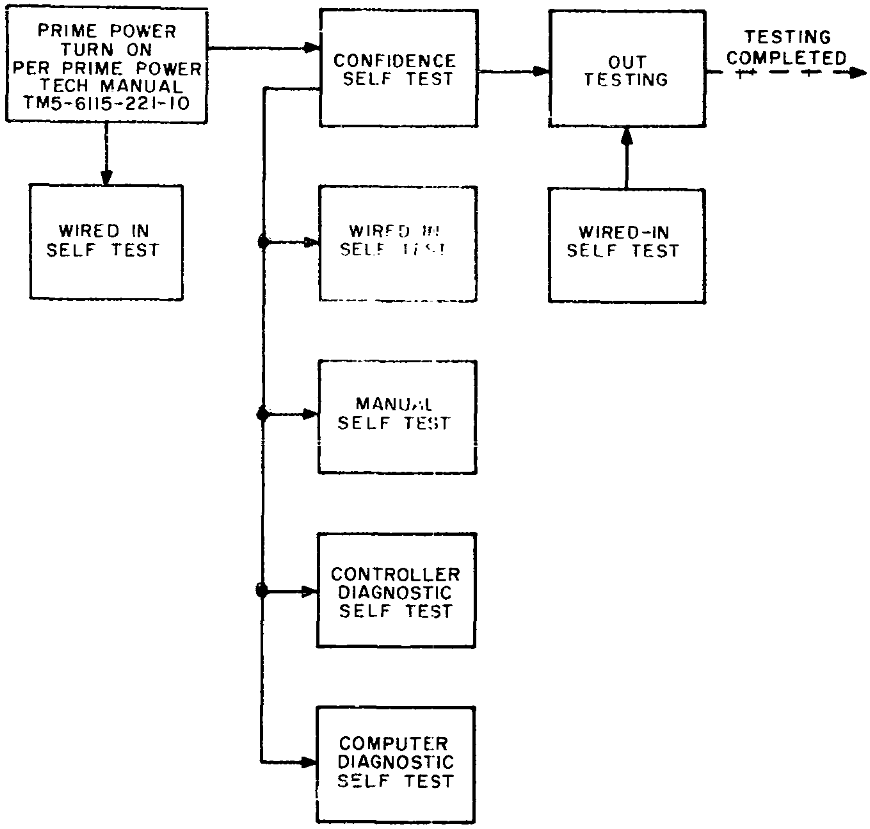


Figure 3-3. Operational procedure for in-process self test and fault isolation

Figure 3-4 represents the physical configuration of the system to be implemented. Two bus systems will be employed: (1) A hut bus, and (2) A signal ground bus. As shown in Figure 3-4 the rack frames will attach directly to the hut bus, the shield ground bus in each rack (but isolated from the rack) will also connect directly to hut bus. The signal ground buses connect directly to the signal ground hut bus and provide a low resistance path for DC return currents to the internal power supplies. The primary AC power returns will be carried isolated throughout the system and will be tied to the hut bus at the main distribution point only.

The appropriate hut bus bars in ETG-1 and ETG-2 will be connected to each other. The hut bus will return to earth ground via a stake or stakes driven deep into the earth.

The HTS will use the same type grounding system and will be separated from the ETS. When it is necessary to combine HTS and ETS to test a UUT, then the HTS hut bus will connect to the ETS hut bus at the earth ground point.

(1) Chassis: The chassis will be connected to Pin No. 26 of the power plug only and will not be used for electrical ground. (Figure 3-5 Insert A.)

(2) Each chassis will contain an isolated signal ground bus which will connect through appropriate pins in the power plug to the rack signal ground bus. All signal grounds from each circuit card will run directly to chassis signal ground bus and not to the next card. (Figure 3-5 Insert B.)

(3) Shields within a chassis will be tied at one end only and connected through the power plug to shield ground bus (applies to shields not being used as returns). See Figure 3-5, Insert C.

(4) Coax cable shields used at frequencies above 100 KC will be tied at both ends but will run isolated in connectors. (Figure 3-5 Insert D.) If coax or shielded wire (shield used as return) is employed at lower frequencies, then signal ground connection will be made at one end only.

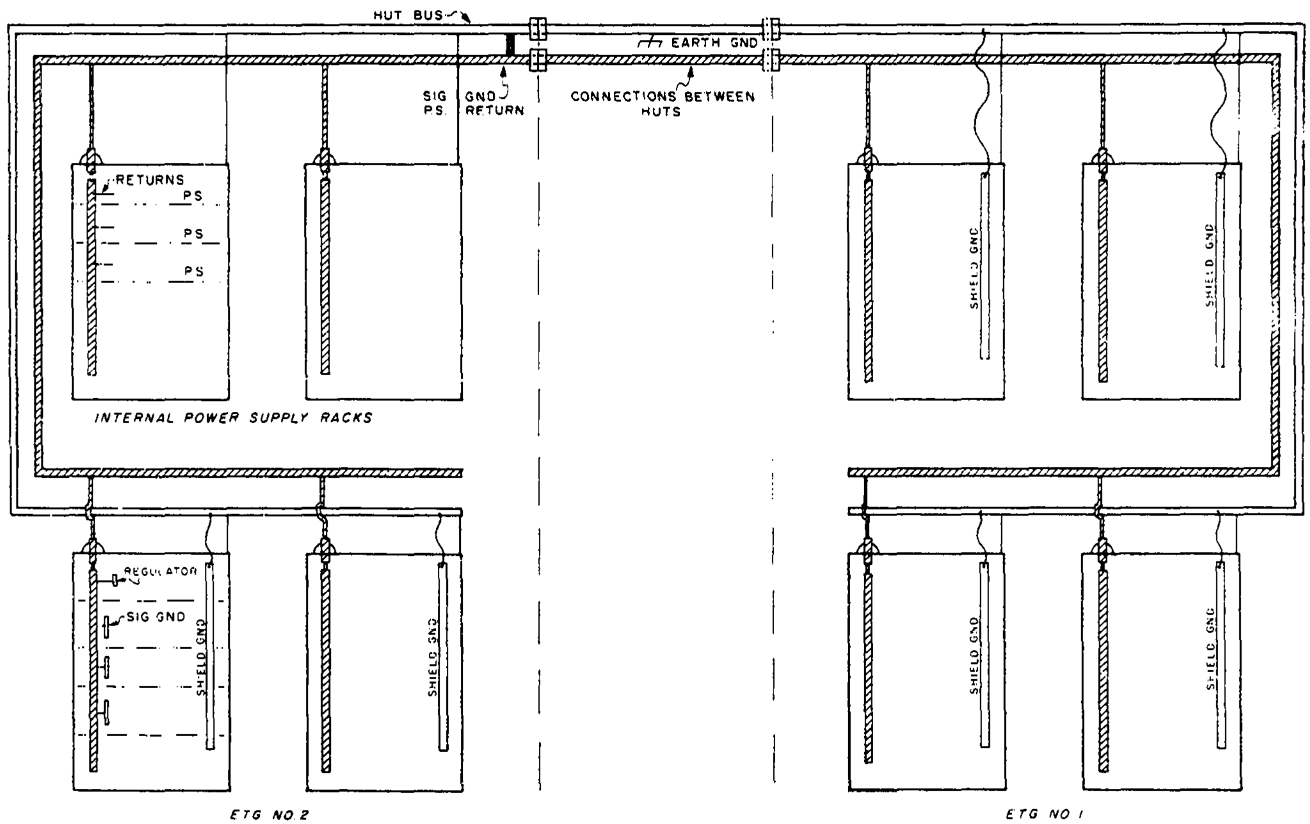


Figure 3-4. Physical configuration of MTE grounding system

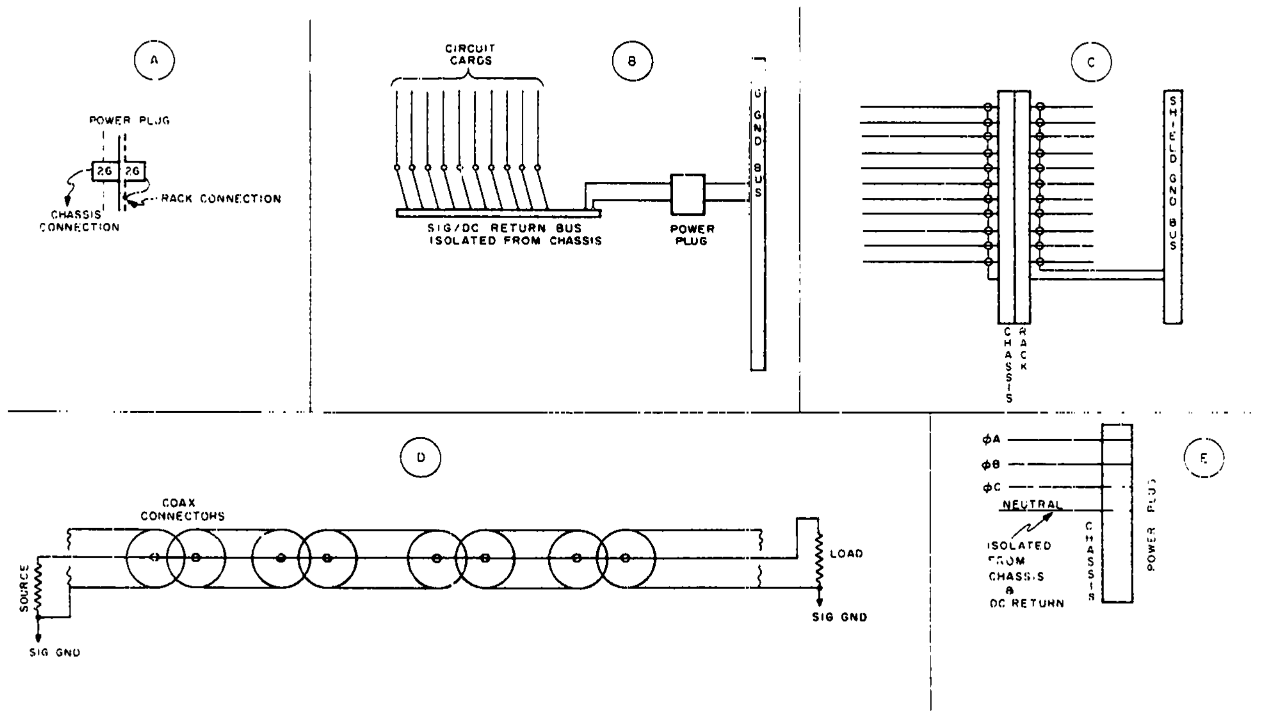


Figure 3-5. Equipment grounding details

(5) AC return or neutral will not tie to any other ground in the chassis but will remain completely isolated. (Figure 3-5, Insert E.)

(6) All chassis that provide a stimulus to a UUT or make a measurement directly from a UUT will use the UUT signal ground as reference, causing the appropriate input or output circuits to be isolated.

SECTION 4

STANDARDS DESIGN AND DEVELOPMENT

4.1 STANDARD CIRCUITS

4.1.1 STANDARD CIRCUITS PROGRESS

During the past quarter, the standard circuits group has designed and released for production 18 types of millimodules and 16 types of millimodule boards. This effort includes the modification of seven of the nine millimodule circuits described in the MTE Third Quarterly Interim Technical Report to meet increased system requirements and completes the design of all standard circuits and boards for which requirements presently exist. The objective was to satisfy system requirements with the minimum number of standard building block circuits and boards.

Standard Nomenclature, Ordnance numbers, and other pertinent data for these Standard Millimodules and Standard Millimodule boards are given in Section 4.1.5.

4.1.2 STANDARD CIRCUIT DESIGN PHILOSOPHY

A. Worst Case Design

All standard circuits have been designed against "Worst Case" conditions, entailing the use of maximum tolerance conditions of components as well as the derating of transistor current gain (Beta) by 25% - 30% to ensure operation at low temperature and end-of-life conditions. All circuits have been tested over the ambient temperature range -55°C to +115°C to prove that no marginal operating conditions prevail over the normal operating temperature range of -20°C to +70°C.

B. Noise Immunity

A two volt level of immunity to noise has been designed into seven of the digital circuits. These circuits are those most often used within the MTE system to send or receive digital information over long lines. Diode clamping has been incorporated on the output of all digital circuits in order to provide a low source impedance at the binary "1" level.

C. Basic Logic

The standard circuits developed for the MTE system all make use of one or the other of two basic types of logic:

(1) The MTE standard circuits which make use of NAND gate logic where
a binary "1" = +6.7 volts and
a binary "0" = 0 volts.

(2) The MTE standard circuits internal to the computer which make use of resistor-coupled transistor logic where
a binary "1" = 0 volts and
a binary "0" = -3.7 volts.

D. Standard Loads

The standard unit load for the MTE standard circuit is a single NAND gate input requiring a maximum current of 3.8ma to be actuated. The standard unit load within the computer is the transistor gate requiring a maximum current of 0.7ma to be actuated.

4.1.3 STANDARD CIRCUITS

A. Circuit List

A list of the standard circuits developed for the MTE system is given below, followed by a brief description of each.

MTE Standard Circuits

(1) NAND Gate, 1Mc

(2) NAND Gate, 10Mc

(3) Flip-Flop, 1Mc

(4) Flip-Flop, 10Mc

(5) Power Amplifier/Line Driver

(6) Power Inverter/Line Driver

(7) Trigger, 1Mc

(8) Trigger, 10Mc

(9) Diode Cluster

(10) Relay/Lamp Driver

(11) Exclusive NOR

(12) Comparator

(13) 4 Gate

(14) Gated Amplifier

(15) NOR Gate

(16) Gated Flip-Flop

(17) XY Driver

(18) Inhibit Driver

B. MTE Standard Circuits

a. NAND Gate

The NAND Gate has been designed to perform logical NAND operations within the MTE system. The truth table and symbol for this device are shown in Figure 4-1.

The medium speed (1Mc) and high speed (10Mc) NAND Gates are identical in design except for the respective transistors and associated collector resistors. The circuit has been designed to operate from either level or pulse inputs; and each millimodule contains two such gate circuits.

In this circuit, Binary "0" = +0.20V ±0.15V.
and Binary "1" = +6.7V ±0.6V.

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

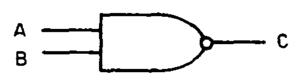
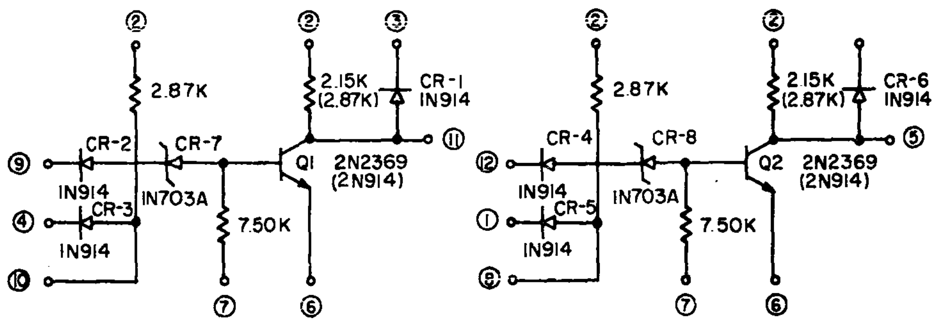


Figure 4-1. NAND gate truth table and symbol.



NOTE: NUMBERS IN PARENTHESIS ARE USED IN THE MEDIUM SPEED (IMC) UNIT.

KEY : PIN 2 = +12V PIN 6 = GND
PIN 3 = +6V PIN 7 = -6V

Figure 4-2. NAND gate schematic.

The NAND Gate performs a gating and amplifying function. Referring to the circuit diagram of Figure 4-2, each of the two circuits in the millimodule is identical and the gating function is done by the input diodes CR-2 and CR-3 (CR-4 and CR-5) when the cathode of either of these diodes is at ground potential (binary "0") that diode conducts and the anode is approximately at ground potential. Zener diodes CR-7, (CR-8) perform a level shifting operation causing the base of transistor Q1 (Q2) to be negative. This negative potential turns the transistor off; when the transistor is off, the output is clamped by diode CR-1 (CR-6) to approximately +6.7 volts (binary "1"). In the other state, when +6.7 volts (binary "1") is placed on the cathodes of the input diodes, these turn off and the transistor turns on. The transistor saturates and the output is clamped to ground potential (binary "0"). The NAND Gate can drive up to 6 gate loads.

b. Flip-Flop

The Flip-Flop has been designed to store binary information. The medium speed (1Mc) and high speed (10Mc) Flip-Flop circuits are identical except for the transistors and value of the associated collector resistors.

The Flip-Flop consists of two NAND gates placed back-to-back. There are two sets of inputs to the Flip-Flop, a control input and a complementing input. The control input is driven by a voltage level and delivers a voltage level to the Flip-Flop; while the complementing input changes this voltage swing to a pulse (CRD Gate), which triggers the Flip-Flop. A binary "0" to either input while the others have binary "1"s will set that Flip-Flop side to a "1".

The logic symbol for the Flip-Flop is shown in Figure 4-3 and the circuit is shown in Figure 4-4. The circuit can drive up to 5 gate loads. Pins 8 and 10 have been brought out in order that additional diodes may be connected to the circuit to perform logical NAND operations.

c. Line Drivers

The NAND Gate and Flip-Flop circuits described above, can drive a maximum of 6 loads and cannot drive a line external to the rack. In MTE there is the

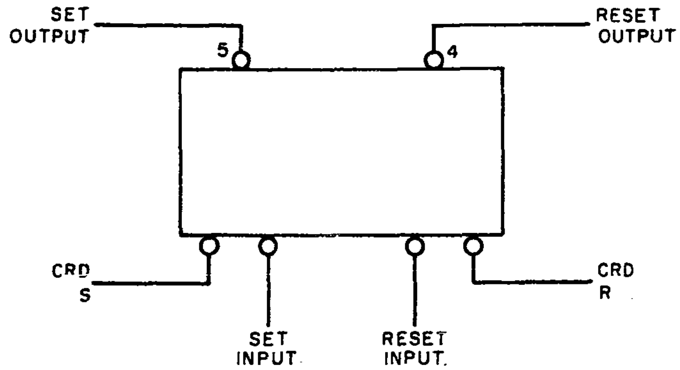
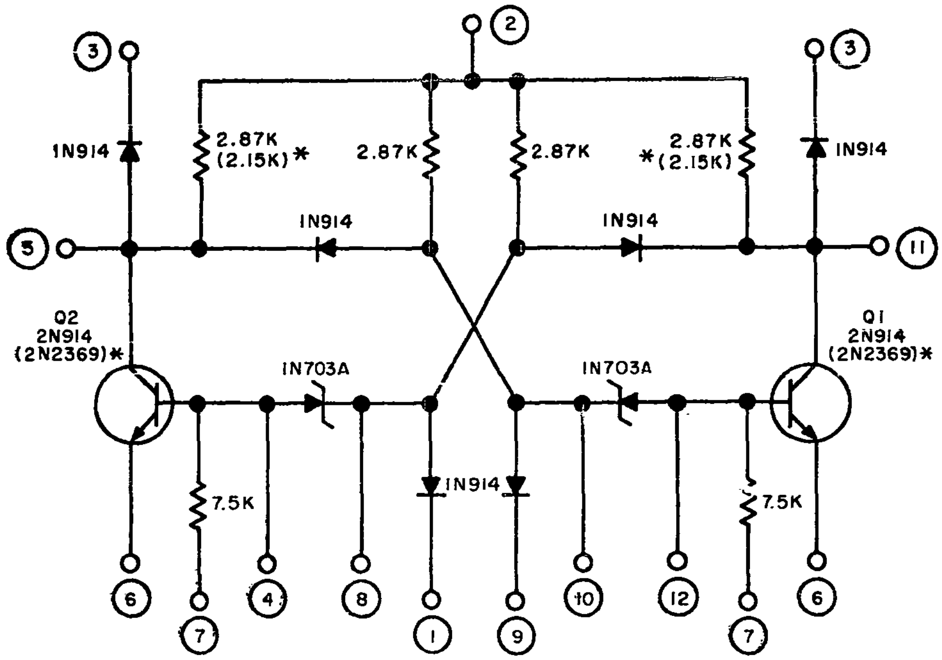


Figure 4-3. Flip flop logic symbol



*NOTE : NUMBERS IN PARENTHESES ARE USED IN THE HIGH-SPEED (10MC) UNIT KEY:

PIN 2: +12V	PIN 4: CRD S
PIN 3: +6V	PIN 12: CRD R
PIN 6: GROUND	PIN 1: SET INPUT
PIN 7: −6V	PIN 9: RESET INPUT
PIN 5: SET OUTPUT	PIN 8: SET NODE
PIN 11: RESET OUTPUT	PIN 10: RESET NODE

Figure 4-4. Flip flop schematic.

requirement of driving as many as 10-25 loads simultaneously; in addition, many signals must be transmitted from 50-75 feet. These two requirements must be accomplished both with and without signal inversion. The Power Amplifier/Line Driver and Power Inverter/Line Drivers were designed to meet these requirements. Schematics of these line driver circuits are shown in the Figures 4-5 and 4-6. Two units (either two Power Amplifier or two Power Inverter Line Drivers) are packaged in a millimodule.

Input diode clusters can be added to the input of either circuit to provide gating operation. Input loading is a maximum of one gate load.

A line driver can drive 25 gate loads and/or 2500 μμfd of line capacity at a maximum repetition rate of 250 kc. The repetition rate can be increased at reduced loading such that the driver can be operated at 1Mc with 5 gate loads and 300 μμfd of capacity.

d. Trigger

The trigger has been designed to perform gating and steering operations when used in conjunction with the standard Flip-Flop. The medium speed (1Mc) and high speed (10Mc) Trigger circuits are identical except for the diode across the resistor in the high speed circuit.

The standard millimodule contains four identical trigger circuits. The logic symbol and schematic diagram are shown in Figures 4-7 and 4-8.

The trigger operates by differentiating a negative-going voltage, providing a pulse to trigger the flip-flop. The resistor is used as a steering gate to determine which side of the flip-flop will be triggered. The resistor output can be connected to the output of its own flip-flop, or it can be steered from some other source to accomplish special logic functions.

The trigger, when used with the flip-flop, presents a 1 1/2 gate load.

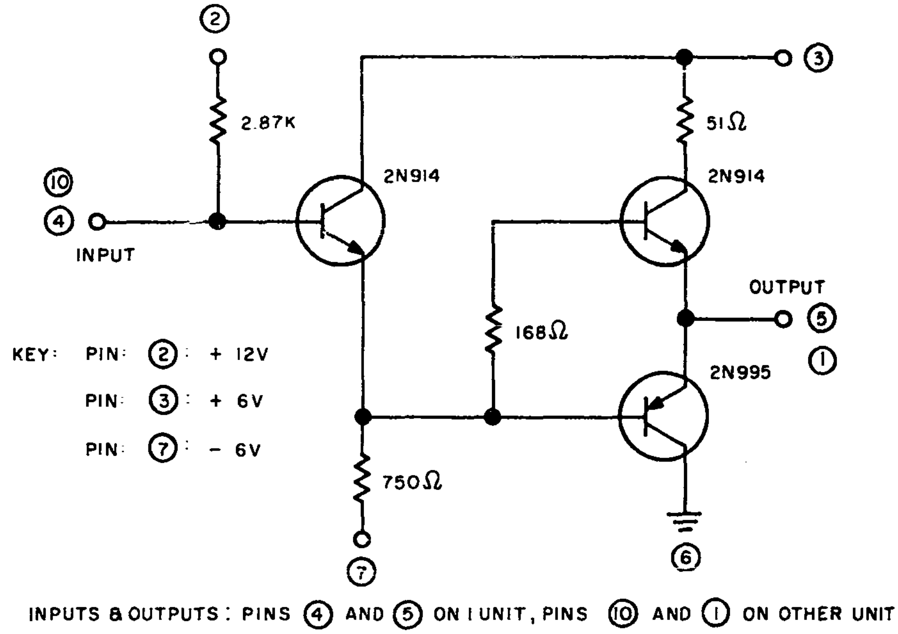


Figure 4-5. Power amplifier/line driver - 2 per millimodule.

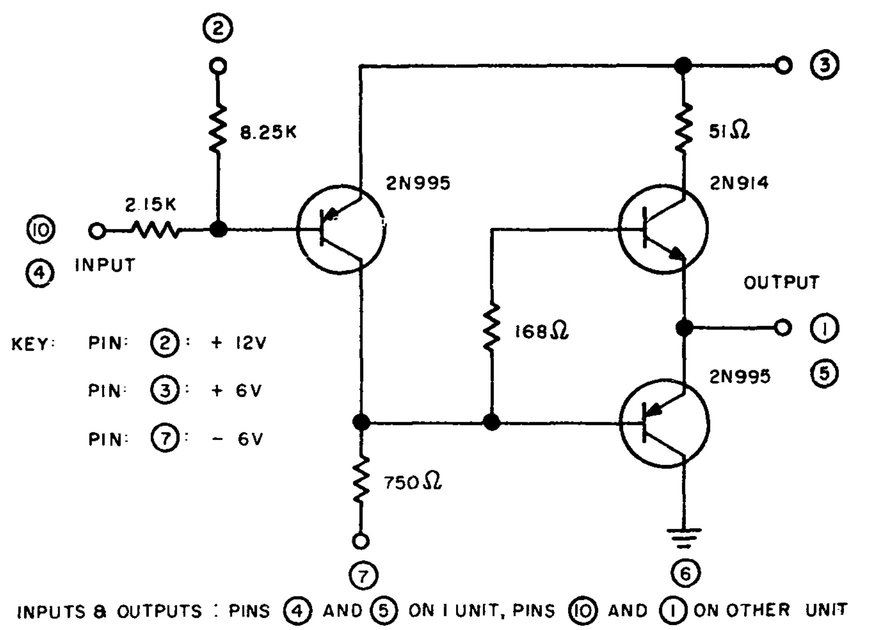


Figure 4-6. Power invertor/line driver - 2 per millimodule.

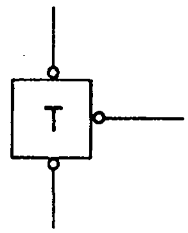
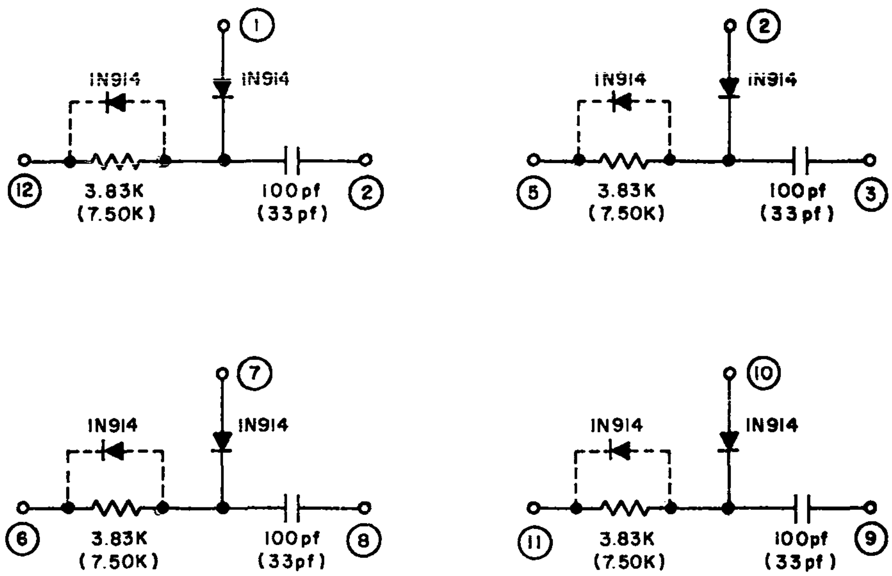


Figure 4-7. Trigger logic symbol



NOTE: NUMBERS IN PARENTHESES AND DIODES DOTTED IN ARE USED IN THE HIGH SPEED (10mc) UNIT.

Figure 4-8. 1 Mc trigger millimodule.

e. Diode Cluster

The Diode Cluster circuit remains as discussed and illustrated in the MTE Third Quarterly Interim Technical Report.

f. **Relay/Lamp Driver**

The Relay Driver described in the Third Quarterly Interim Technical Report was re-designed during this reporting period. The re-design incorporates into one circuit, gating and driving requirements of both relays and lamps. In addition, input loading has been minimized, buffering is provided between input and output, and a separate ground return is provided at the output to isolate relay and lamp returns from signal ground.

The combination relay/ lamp driver is a non-inverting driver containing a diode "AND" input diode cluster, and a node input for additional diode gating inputs. The logic symbol and truth table for the relay/lamp driver are shown in Figure 4-9.

Referring to the schematic of Figure 4-10, the circuit performs both a gating and driving function and operates from either level or pulse inputs. The gating function is performed by the input diodes CR-1 and CR-4. When the cathode of either of these diodes is at ground potential (binary "0") that diode conducts and the anode side of the diodes assumes approximately ground potential. Diodes CR-2 and CR-3 perform level-shifting operation causing the base of transistor Q2 to become negative. Q2 thus is turned off. Transistor Ql is an emitter follower and buffers the input from the driving transistor Q2. In the other state, when +6.7 volts (binary "1") is placed on the cathodes of all input diodes, these diodes will turn off and the driving transistor Q2 will be turned on and will saturate.

g. Exclusive NOR

This circuit provides a logical "1" output when the two input signals are different, and a logical "0" when both signals are the same. The truth table and logic symbol for the circuit are shown in Figure 4-11.

IN		OUT
A	B	C
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

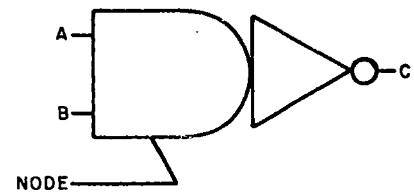


Figure 4-9. Truth table and logic symbol for relay/lamp driver

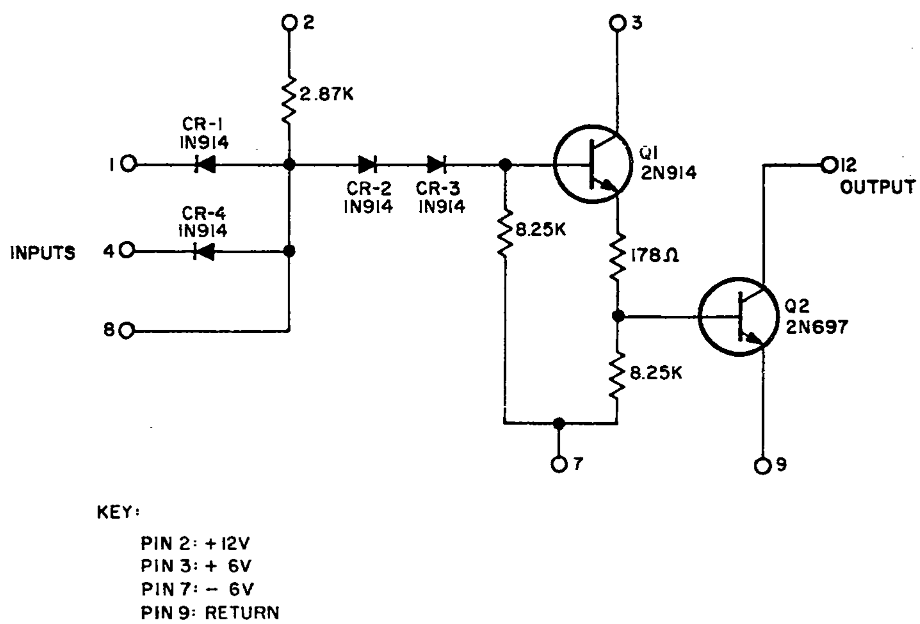


Figure 4-10. Schematic - relay/lamp driver.

A	B	OUTPUT ($\overline{C}$)
1	0	1
0	1	1
0	0	0
1	1	0

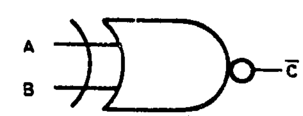


Figure 4-11. Truth table and logic symbol - exclusive NOR.

The frequency of operation of this circuit is limited to 1Mc and will typically be less than 100KC. The circuit (Figure 4-12) consists of three NAND gates connected so as to give an exclusive NOR.

h. Comparator

The comparator circuit is used to compare the outputs of two flip-flops. The comparator circuit output is +6.7 volts if the two flip-flops are in the same state, and 0 volts if the flip-flops are not in the same state. Figure 4-13 shows the schematic of the comparator circuit, which consists of three separate circuits externally interconnected as shown by the dotted lines.

If the set sides of both flip-flops are at binary "0", point (a) is clamped to ground, point (b) is clamped to +6.7V, diode D-5 is reverse biased, and the output (pin 12) is clamped to +6V. If one set side is at binary "1" while the other is at binary "0", points (a) and (b) will both be clamped to +1V. and the output pin will be clamped to 0V. The comparator circuit has no drive capability and must be buffered by a special circuit.

C. MTE Computer Standard Circuits

Four digital circuits have been re-designed in millimodule form to perform the basic digital operations of the MTE Computer. The circuits use the same principles laid down in the design of the RCA AM 3100 and 3200 computers, namely:

(a) The use of complementary transistors to keep power consumption to a minimum,
(b) The use of [illegible]-coupled transistor logic, and
(c) The use of no reactive elements.

One improvement incorporated into these circuits was the reduction of the supply voltages by a factor of two with the component values remaining the same. This resulted in a reduction of power consumption by a factor of four. The logic levels of these circuits are as follows:

Binary "0": -3.65V ±0.4V.
Binary "1": -0.15V ±0.1V.

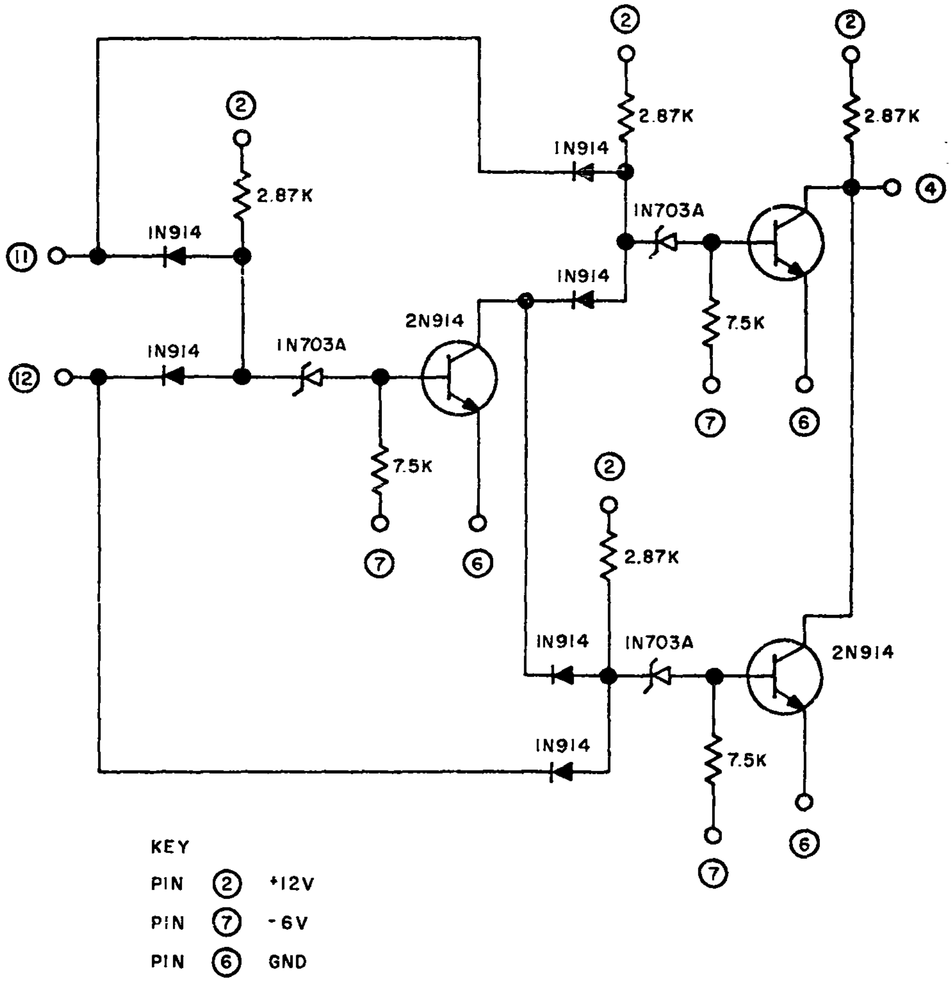


Figure 4-12. Schematic diagram - exclusive NOR.

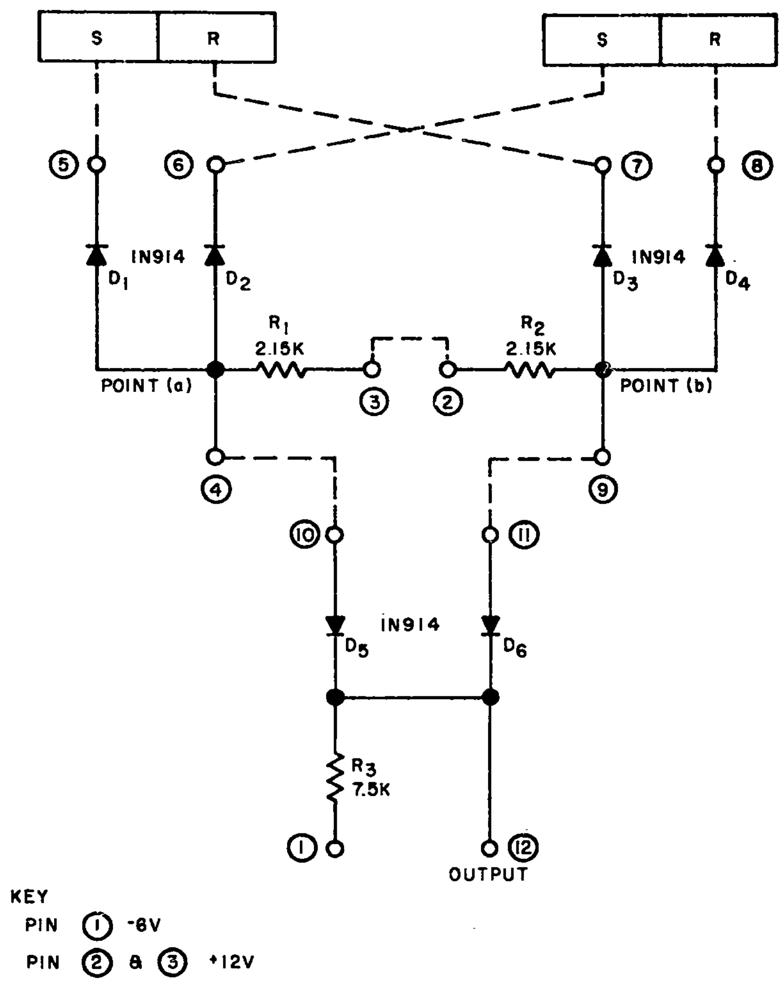


Figure 4-13. Schematic - comparator millimodule.

A brief discussion of the four basic digital circuits and of two computer memory circuits follows:

a. Four Gates

The gating functions for the MTE computer are accomplished by means of saturated transistor switches. A single transistor performs a single gating function. Connecting transistors in series causes logical "AND" operations to be performed; while connecting transistors in parallel cause logical "OR" operations to be performed. Typical "AND" and "OR" configurations are shown in Figure 4-14.

Transistors may be placed both in series and parallel combinations in order to perform complex "AND" and "OR" operations. A maximum of 6 gates may be placed in series to perform "AND" operations, while a maximum of 5 gates may be placed in parallel for "OR" operations.

A Gate Millimodule contains four circuits which may be connected in any required manner. The schematic is shown in Figure 4-15.

b. Gated Amplifier

The Standard Computer Gated Amplifier Circuit uses a saturating switch which performs logical inversions. It is designed to operate at repetition rates up to 2Mc. This circuit can also be used as a buffer in order to obtain a fan-out to a large number of loads. The input to this circuit is gated by standard transistor gate circuits.

The schematic diagram of the Gated Amplifier Millimodule is shown in Figure 4-16. In addition to the saturating switch, the circuit contains an NPN transistor (Q2) to speed-up the destoring of the PNP transistor Q3. This NPN transistor guarantees a fast and predictable turn-off over the required temperature range. An additional transistor collector resistor (R7) is also contained in the millimodule; this may be connected in parallel with R5 to ensure a fast discharge of any load capacitance which may be present due to long lines and small loads.

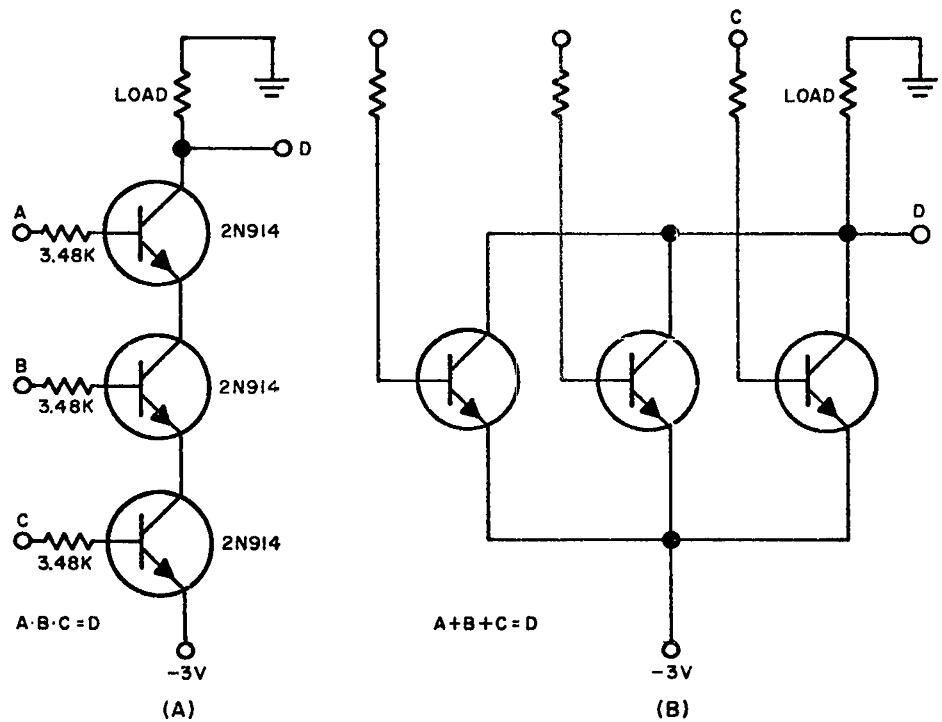


Figure 4-14. Typical AND and OR configurations.

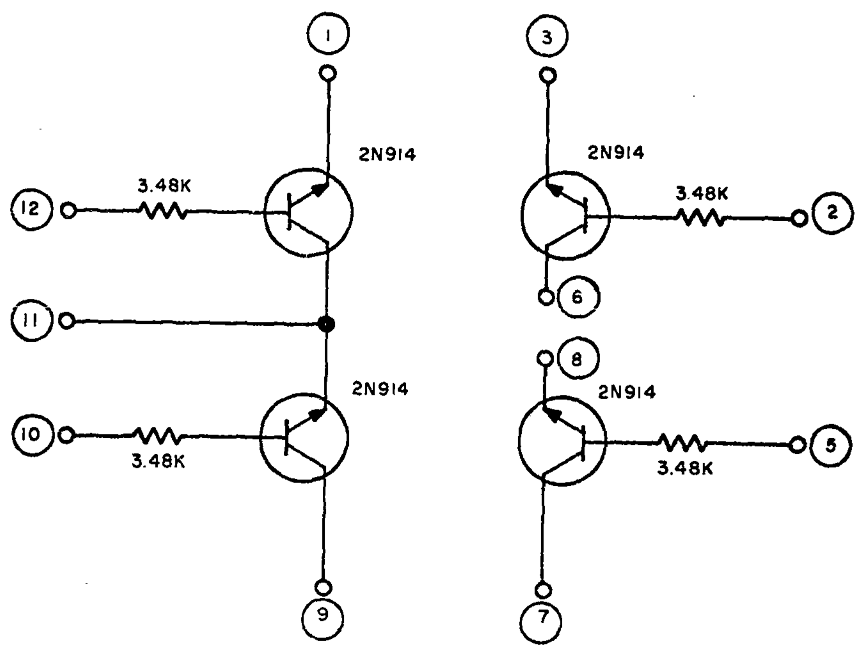


Figure 4-15. Four gate millimodule schematic.

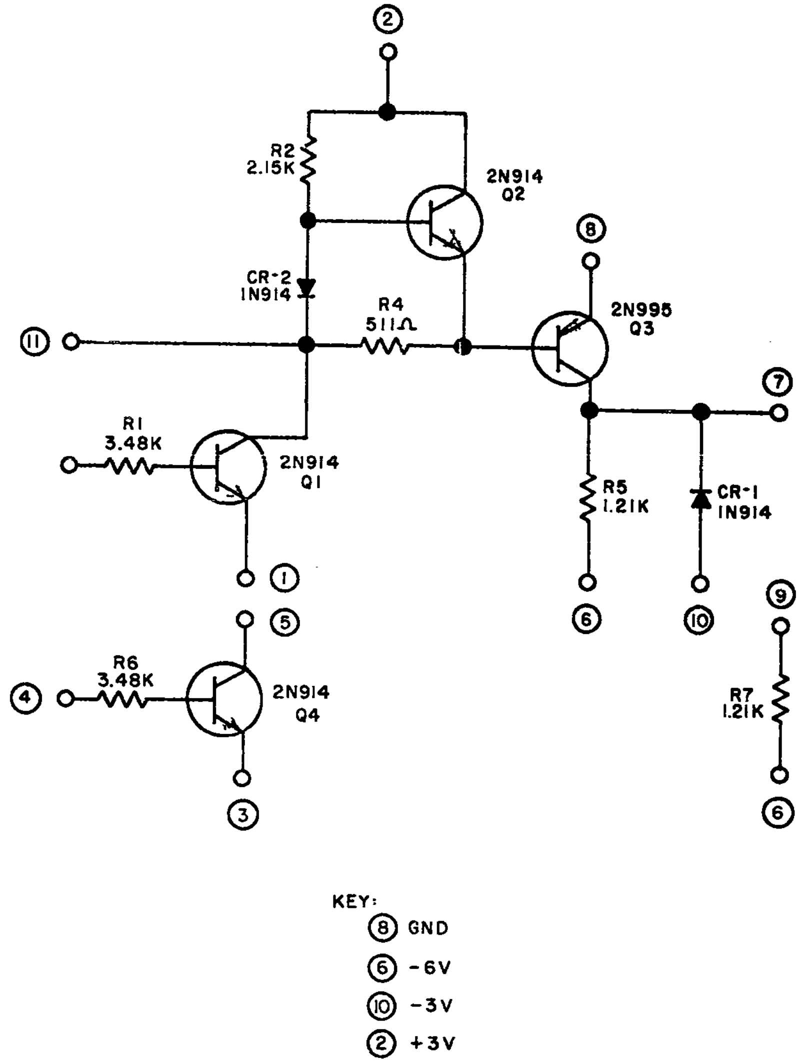


Figure 4-16. Schematic - computer gated amplifier.

c. NOR Gate

The NOR Gate millimodule used in the MTE Computer is a saturating, high-speed gate. It is designed to have a pair delay of 90 nanoseconds or less over the temperature range of -20°C to +75°C.

This circuit was designed primarily to perform the high speed carry propagation in the computer. The logic to generate these carries consists of 15 pair delay which must be generated within 1. 5 microseconds. Each NOR Gate Millimodule contains one pair of NOR gates.

The NOR Gate was designed using a pair of special diodes (stabistors) (CR-3, CR-4 and CR-7, CR-8) instead of a resistor and capacitor, to couple the signal to the base of the transistor. The addition of these stabistors reduces the loading which this circuit represents to a flip-flop or a gated amplifier, as well as increasing the FAN-OUT capability and speed of the circuit.

The Schematic Circuit of the NOR Gate Millimodule is shown in Figure 4-17.

d. Gated Flip-Flop.

The Gated Flip-Flop used in the MTE Computer is a saturating flip-flop using transistor gates for steering. It is designed to operate at a repetition rate up to 2Mc over the temperature range of -20°C to +75°C.

The circuit can be used as a counter, shift register, or control flip-flop by proper interconnection of the transistor gating inputs.

This flip-flop consists of two grounded emitter amplifiers (Q1 and Q3) with the output of each tied to the input of the other. The outputs of each side of the flip-flop (pins 7 and 9) are clamped through a diode to the -3 volt supply. Two gated inputs to the flip-flop (Q2 and Q4) are provided within the millimodule. Additional gated inputs may be added to the flip-flop in order to form logical "AND" and "OR" functions. These additional logical functions may be obtained by using the Four Gate millimodule and connecting those transistors in the appropriate manner to pins 1, 3, 5 and 11 of the Gated Flip-Flop.

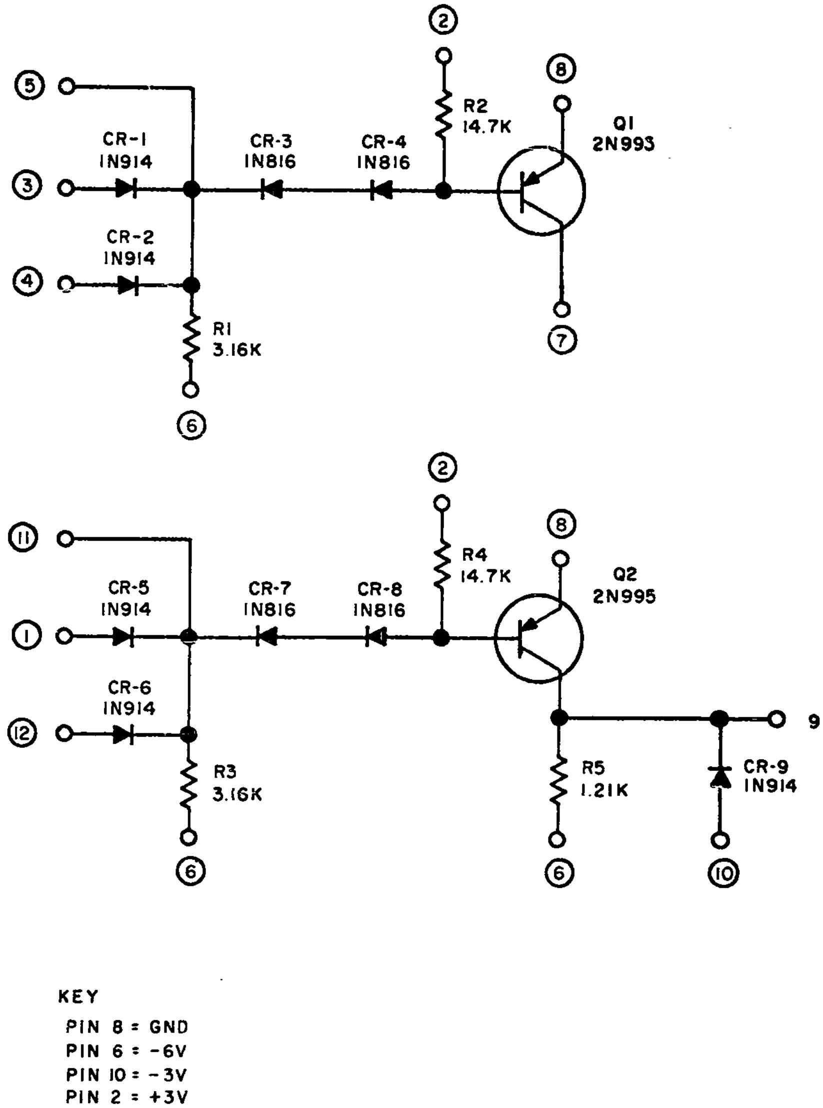


Figure 4-17. Schematic - NOR gate millimodule.

The Schematic of the Gated Flip-Flop is shown in Figure 4-18.

e. XY Driver

The XY Driver circuit, used in the MTE Computer, is a saturating switch which can be used to generate either the read or write half-current pulses. This circuit is designed to operate with a memory cycle time of 12 microseconds over the temperature range -20°C to +75°C. The circuit is designed to be pulsed by a standard gating chain. The pulse from the gating chain is AC-coupled to the output transistor by means of transformer T1. The output transistor (Q2) will supply or absorb the 290ma half-current drive which is required during the read and write modes. To improve the recovery time of the transformer, the resistor R3 and the diode CR-1 were added to the circuit.

The schematic diagram of the XY Driver Millimodule is shown in Figure 4-19.

f. Inhibit Driver

The Inhibit Driver Millimodule, used in the MTE Computer, is a saturating switch which will generate the inhibit current for an entire plane within the ferrite core memory. The Inhibit Driver circuit is designed to operate at a memory cycle time of 12 microseconds over the temperature range of -20°C to +75°C.

This circuit, like the XY Driver, is designed to be pulsed by a standard gating chain. However, in this case the pulse from the gating chain is direct-coupled to the output stage (Q4). Because of the long storage time associated with the output transistor (Q4) a destoring transistor (Q3) was added to the circuit. The addition of this destoring transistor results in a short and very predictable turn-off time of the output transistor.

The schematic diagram of the Inhibit Driver Millimodule is shown in Figure 4-20.

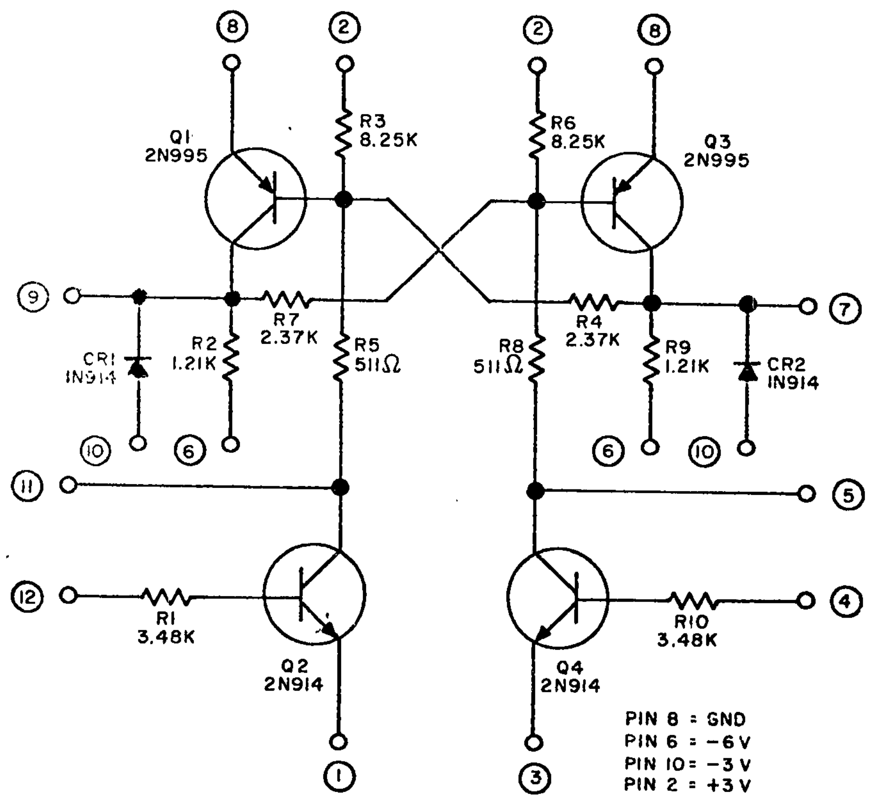


Figure 4-18. Schematic - gated flip-flop.

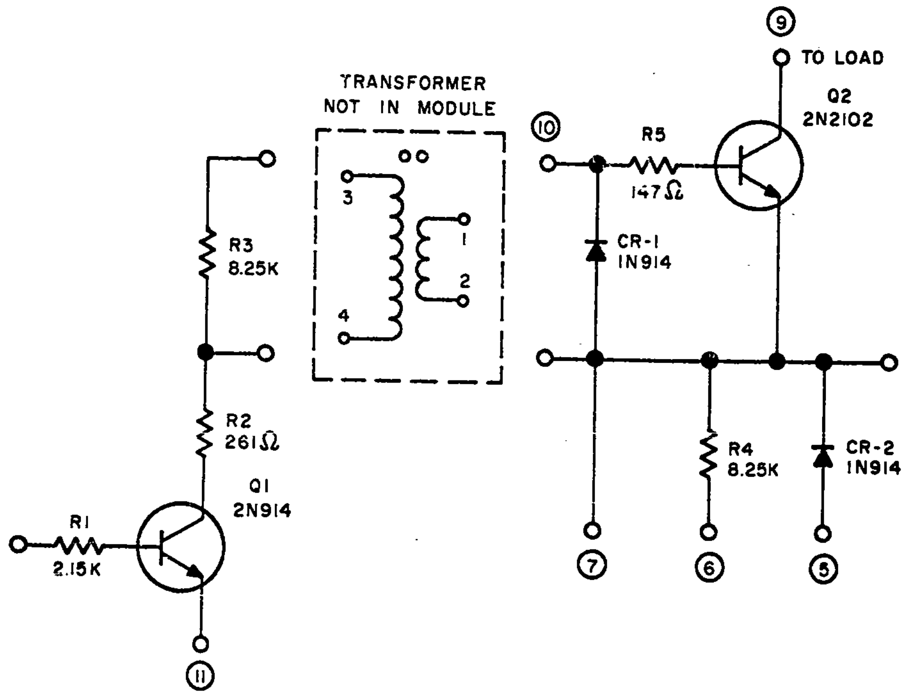


Figure 4-19. Schematic - XY driver.

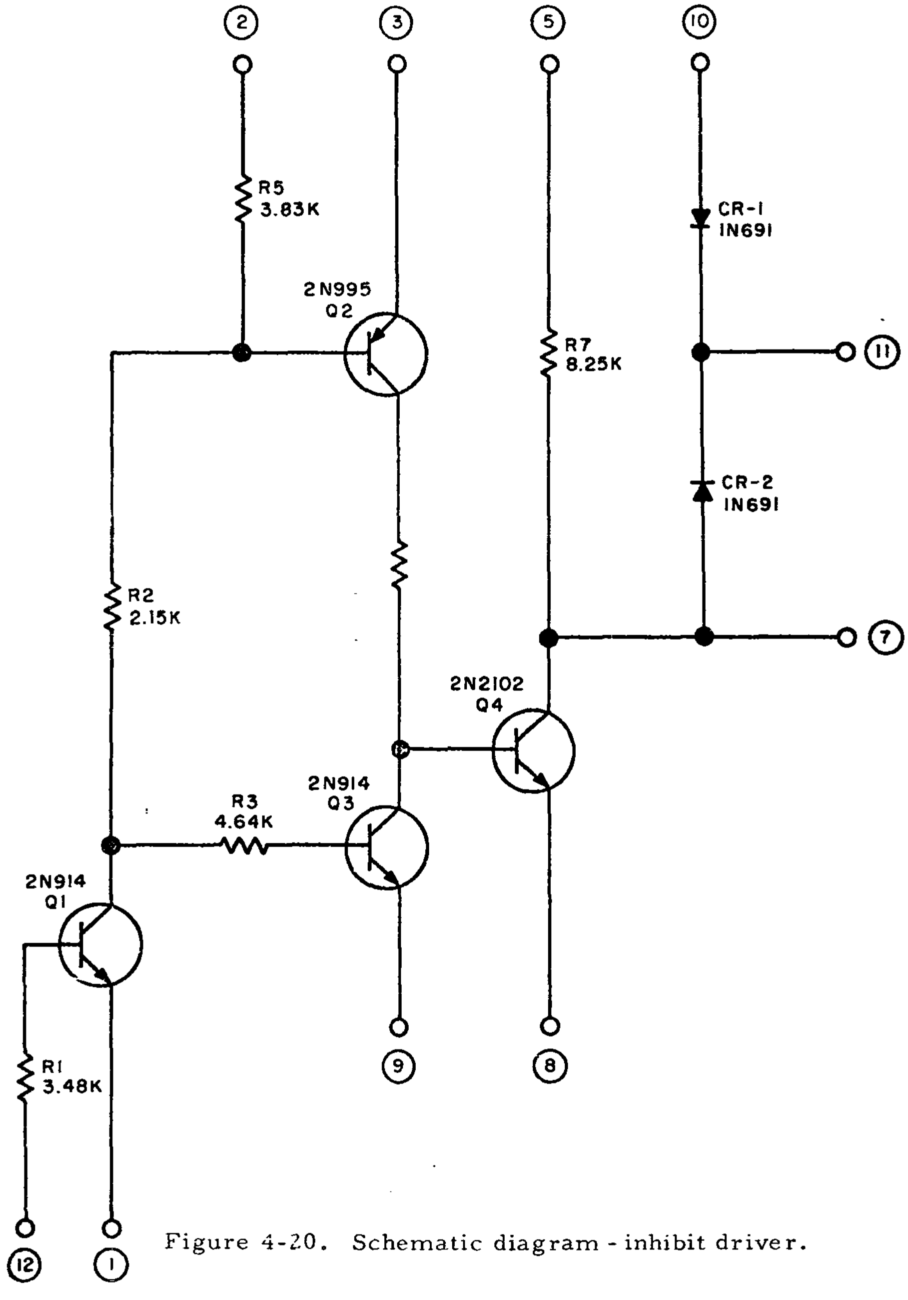


Figure 4-20. Schematic diagram - inhibit driver.

4.1.4 STANDARD CIRCUIT BOARDS

A. General

Standard Millimodule circuits are mounted on circuit boards in certain logical configurations to form standard functional boards. The following thirteen standard boards were designed during this report period; the purpose and circuit composition of each is briefly described:

(1) Address/ Storage Board
(2) Address/Sub-Address Board
(3) Three Character Storage Board
(4) Two Character Storage Board
(5) Up Counter Board
(6) Down Counter Board
(7) Driver Relay Board
(8) Relay/Lamp Driver Board
(9) Decimal Decoder Board
(10) Inverter/Gate Board
(11) Serial/ Parallel Shift Register Board
(12) Line Driver/Power Amplifier Board
(13) Line Driver/Power Inverter Board

B. Circuit Board Descriptions

a. Address/Storage Board

The Address/Storage Board consists of 7 gate, 2 diode cluster, 5 power amplifier, 2 power inverter, and 6 flip-flop modules. The function of this board is to route timing signals to the BCD character storage board under control of the Switching Control Buffer. These signals enable BCD information to be transferred to and stored in the character board from the registers of the Switching Control Buffer. The Address/Storage Board has three main logic functions - address logic, sub-address logic, and BCD character storage logic.

b. Address/Sub-Address Board

The Address/Sub-Address Board consists of 9 gate, 4 power inverter, 1 power amplifier, 4 diode cluster, and 2 flip-flop millimodules. This board is similar in function to the address/storage board, having two main logic functions - address logic and sub-address logic.

c. Three Character Storage Board

The three character storage board consists of 6 gate, 12 flip-flop, and 3 diode cluster millimodules. The function of this board is to receive and store three BCD characters from the Switching Control Buffer. This board can also be used as a four octal character storage board.

d. Two Character Storage Board

The two character storage board consists of 4 gate, 8 flip-flop, 2 diode cluster, and 8 power amplifier millimodules. The function of this board is to receive and store two BCD characters from the Switching Control Buffer.

e. Up Counter Board

The up counter board has two BCD scale-of-ten up counters and consists of 1 gate, 1 diode cluster, 4 trigger, and 8 flip-flop millimodules. The function of this board is to convert the pure binary input to a binary-coded decimal count. The counting sequence is shown in Figure 4-21. The counter counts to 8, as in a standard binary counter, but at the count of 9 an inhibiting action occurs which resets the counter to all zeros.

f. Down Counter Board

The down counter board has two BCD scale-of-ten down counters and consists of 2 gate, 2 diode cluster, 4 trigger, and 8 flip-flop millimodules. The function of this board is to convert pure binary input into a binary coded decimal backward count. The counting sequence is shown in Figure 4-22.

Count	2^3	2^2	2^1	2^0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Figure 4-21. Up Counter Counting Sequence

Count	2^3	2^2	2^1	2^0
0	0	0	0	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1

Figure 4-22. Down Counter Counting Sequence

g. Driver Relay Board

The driver relay board consists of 9 relay/lamp drivers, and 9 relays. Seven SPST, 1 SPDT, and 1 DPDT sets of relay contacts are available from the board connectors. In order to energize a relay, all inputs must be in the logical "1"

condition. The number of possible inputs may be increased by connecting diode clusters to the node connection of the relay/lamp driver millimodule.

h. Relay/Lamp Driver Board

The relay/lamp driver board consists of 12 relay/lamp driver millimodules. The function of the board is to operate up to 12 relays and/or lamps. In order to energize a relay or lamp, all inputs must be in the logical "1" condition. To increase the number of inputs, diode clusters can be connected to the node input of the millimodules.

i. Decimal Decoder Board

The decimal decoder board consists of 10 gate and 5 diode cluster millimodules. The function of this board is to decode any BCD character from 0000 to 1001 into the corresponding decimal number (0 to 9). In order to get a logical "0" at the output, the inputs to the gate must all be in the logical "1" condition.

j. Inverter/Gate Board

The inventer/gate board consists of ten NAND gate millimodules, providing ten 2-input gates and ten 1-input gates. This board is designed to be used with the standard decoder board to obtain the inverse function. The millimodules of this board can also be used as flip-flops by cross-connecting the two-input gates.

k. Serial/Parallel Shift Register Board

This board has two 4-bit registers and consists of 8 trigger and 8 flip-flop millimodules. The function of this board is to transfer information in serial and/or in parallel in the system. The set and reset level controls of each stage are conditioned by the state of the preceding stage. The shift pulse is steered by the level controls to the set or reset side of each stage. Since the level controls of each stage are connected to the outputs of the previous stage, when the shift line is activated, information is shifted to the next stage in the register.

l. Line Drive/Power Amplifier Board

The line driver/power amplifier board consists of 12 power Amplifier/Line Driver millimodules. The function of this board is to transfer pulses and/or levels to many unit loads within a chassis or to loads at a distance in the system.

m. Line Driver/Power Inverter Board

The line driver/power inverter board consists of 12 power inverter/line driver millimodules. The function of this board is to transfer pulses and/or levels to many unit loads within a chassis or to loads at a distance in the system.

4.1.5 STANDARDS NOMENCLATURE

A. Standard Millimodules

M NO.	TITLES	RCA ASSEMBLY	ORDNANCE NUMBER	SCHEMATIC	PHOTO MASTER
M1	Flip-Flop 1 Mc	1733458-501	11076557	1732545	1733863
M2	Flip-Flop 10 Mc	1733458-503	11076558	1732546	1733863
M3	Gate NAND 1 Mc	1733459-501	11076555	1732549	1733864
M4	Gate NAND 10 Mc	1733459-503	11076556	1732550	1733864
M5	Driver, Line/Amp Power	1733460	11076562	1732553	1733865
M6	Trigger, Module 1 Mc	1733461-501	11076559	1732556	1733866
M7	Trigger, Module 10 Mc	1733461-503	11076560	1732557	1733866
M8	Diode, Cluster	1733462	11076561	1732560	1733867
M9	Relay/Lamp Driver	1733463	11076563	1732563	1733868
M10	Driver, Line/Inverter Power	1733843	11076741	1732591	1733870
M11	Flip-Flop, Gated	1733844	11076933	1732594	1733871
M12	Gate, NOR	1733845	11076913	1732597	1733872
M13	Gate, (4)	1733846	11076934	1737100	1733873
M14	Amp, Gated	1733847	11076935	1737103	1733874
M15	Driver, XY	1733848	11076936	1737106	1733875
M16	Driver, Inhibit	1733849	11076937	1737109	1733876
M17	Comparator	1733861	11076932	1737108	1733877
M18	Exclusive NOR	1733842	11076844	1732588	1733869

B. Standard Boards

TITLES	RCA ASSEMBLY	ORDNANCE NUMBER	SCHEMATIC	PHOTO MASTER	MARKING
Driver, Relay	1733472-501	11076861	1733473	1733475	1733476
Driver, Relay/Lamp	1733477-501	11076862	1733478	1733480	1733481
Decoder, Decimal	1733482-501	11076877	1733483	1733485	1733486
Storage, Character (2)	1733487-501	11076878	1733488	1733490	1733491
Storage, Character (3)	1733492-501	11076879	1733493	1733495	1733496
Register, Shift 1Mc	1733497-501	11076880	1733498	1733801	1733802
Register, Shift 10 Mc	1733497-503	11076881	1733499	1733801	1733803
Inverter/Gate 1 Mc	1733804-501	11076882	1733805	1733807	1733808
Counter, Down 1Mc	1733809-501	11076883	1733810	1733813	1733814
Counter, Down 10 Mc	1733809-503	11076884	1733811	1733813	1733815
Counter, Up 1 Mc	1733816-501	11076885	1733817	1733820	1733821
Counter, Up 10 Mc	1733816-503	11076886	1733818	1733820	1733822
Address, Single	1733823-501	11076887	1733824	1733826	1733827
Address, Three	1733828-501	11076888	1733829	1733831	1733832
Driver, Line (Power Inverter)	1733833-501	11076889	1733834	1733837	1733838
Driver, Line (Power Amp)	1733833-501	11076890	1733835	1733837	1733839

4.2 STANDARD PACKAGING DEVELOPMENT

4.2.1 RACK AND CHASSIS DESIGNS

The MTE standard rack and chassis designs were described in the MTE Second Quarterly Interim Technical Report and illustrated in the MTE Third Quarterly Interim Report. The chassis design drawings, updated during this report period, are complete. The rack design drawings have also been updated; however, shock and vibration tests may result in minor modifications to this design.

4.2.2 ENVIRONMENTAL DESIGN TESTS

Initial environmental test effort was begun during the period covered by this report and was concerned with vibration testing of the MTE Standard Rack. The tests were performed at the Dayton T. Brown Co., Bohemia, Long Island.

The locations at the rack at which accelerometers were to be placed were first chosen. The seventeen points chosen (refer to Figures 4-23 and 4-24) were as follows:

(1) Upper right front welded corner - Three directions (x, y, and z)
(2) Right front vertical member (opposite support) - two directions (x and y)
(3) Left front vertical member (between supports) - two directions (x and y)
(4) Right "T" bar (between supports) - two directions (x and y)
(5) Connector panel (between supports) - one direction (x)
(6) Printed circuit board - one direction (x)
(7) Casting (module) - two directions (x and y)
(8) Input (control - base) - three directions (x, y, and z)
(9) Input (verifier - top) - one direction (applied)

Axis directions:

"x" - in the plane running front to rear on the chassis
"y" - in the plane running from side to side on the chassis
"z" - in the plane running the longest dimension of the rack

A one "g" run was made initially for the purpose of evaluating the primary amplification factors; several areas showed amplifications of greater than 2 to 1. With the equipment recalibrated in accordance with the findings of the initial run, the first resonance search was undertaken to the test specifications. Resonant frequencies were found at 23 cps, 175 cps, and 340 cps.

Each resonant point is required to be vibrated for one hour. After approximately four and one-half minutes of vibrating the rack at 23 cps. with an input of 4.5 g's slight circular motions of the front panels was noted. The test was halted and a visual examination of the rack showed hairline cracks in the welded corner joints. The rack corners will be re-welded, strengthened with added corner support, and the tests re-run.

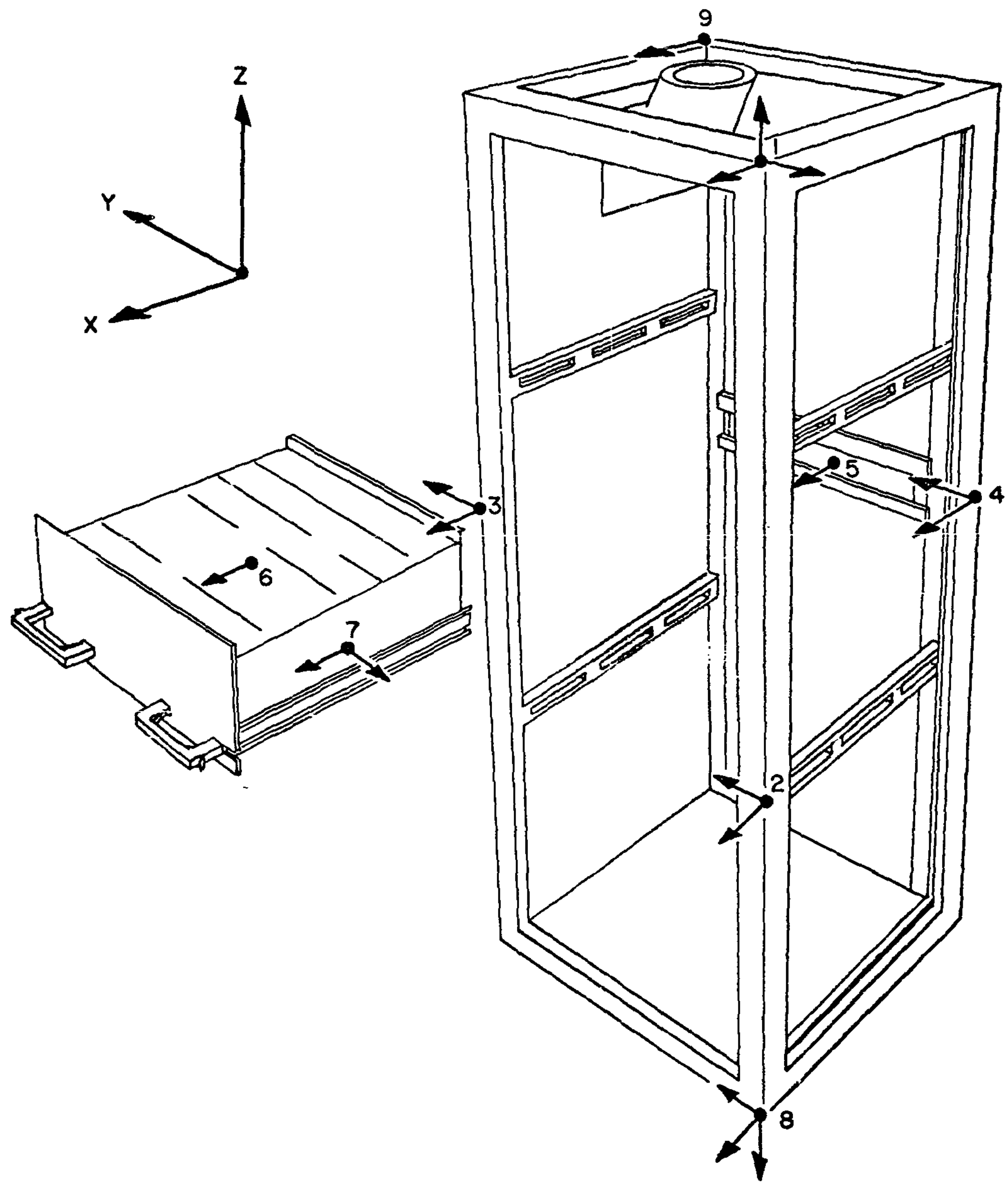


Figure 4-23. Locations of accelerometers on MTE standard rack.

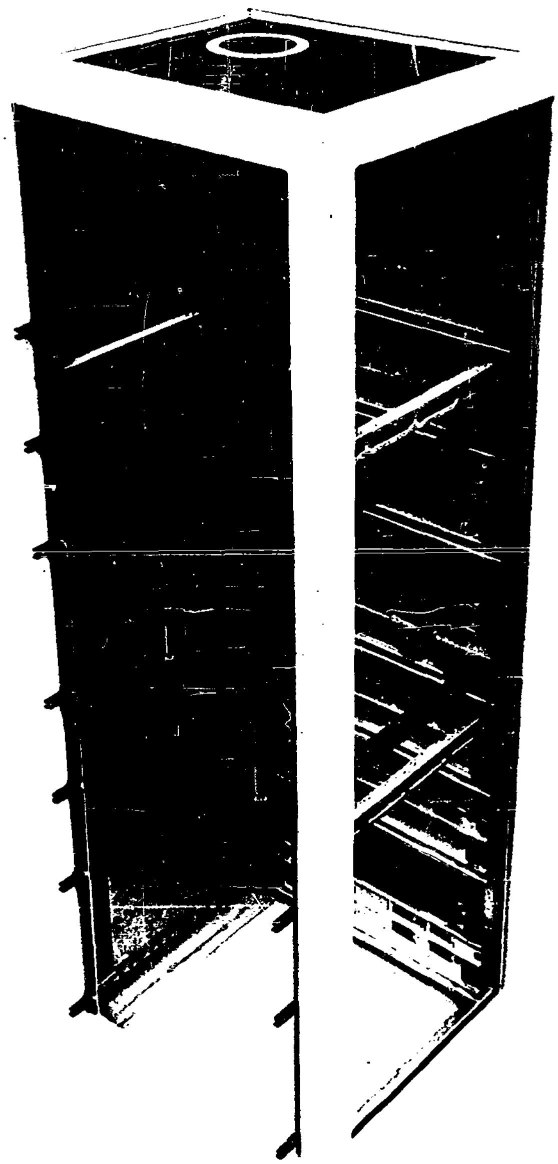


Figure 4-24. Typical rack - drawers removed

4.2.3 COOLING DESIGN TESTS

Design tests were conducted to determine the flow characteristics of the rack plenum and transition piece.

The parallel circuit rack cooling and ventilation system described in the MTE Second Quarterly Interim Technical Report No. CR-62-547-26 has been designed for adequate removal of heat from high density packaged equipment in confined quarters. The intent of this design is to maintain the equipment at a constant temperature level by adequate direction of the cooling air. The air is discharged to the units from small orifices in the plenum. By maintaining pressure differential, of 1 inch water in the plenum, the air can be directed with a sufficient velocity to reach heat dissipating areas with the necessary turbulance to remove this heat. The location and quantity of orifices are governed by the individual unit requirements.

In order to bracket the pressure losses through the rack ducting as an aid to final system balancing, and to investigate the air flow pattern through the plenum, a series of tests has been conducted. Figures 4-25 and 4-26 are typical of the resulting curves for different air entrance conditions into the transition duct. Figure 4-27 shows the air flow pattern through the orifices along the length of the plenum. Since this pattern is relatively constant for the range of required flow rates, and for a coefficient of discharge which was checked at 0.61, the cooling capacity of these orifices was plotted in Figure 4-28.

4.2.4 PLANS

Shock and vibration design verification tests will be performed on the MTE Standard rack and chassis.

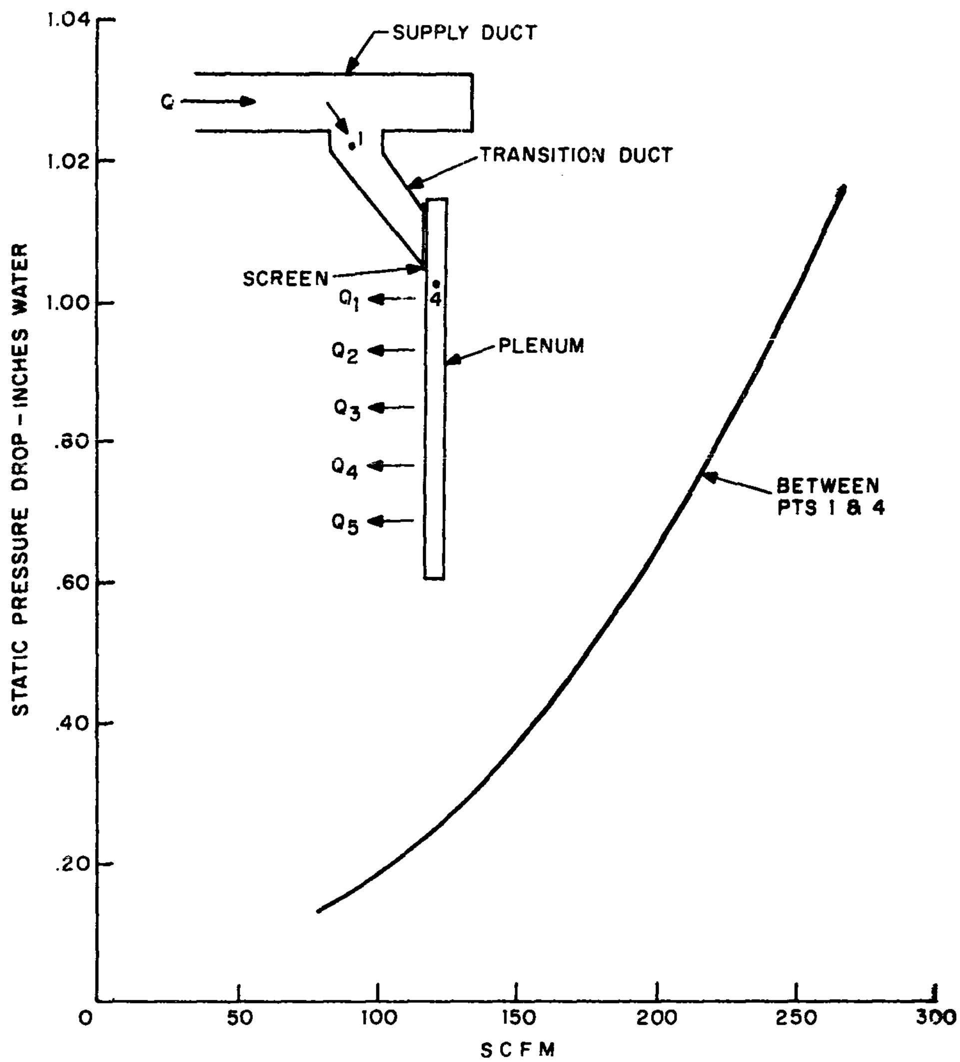


Figure 4-25. Pressure drop vs CFM for rack ducting - condition 1.

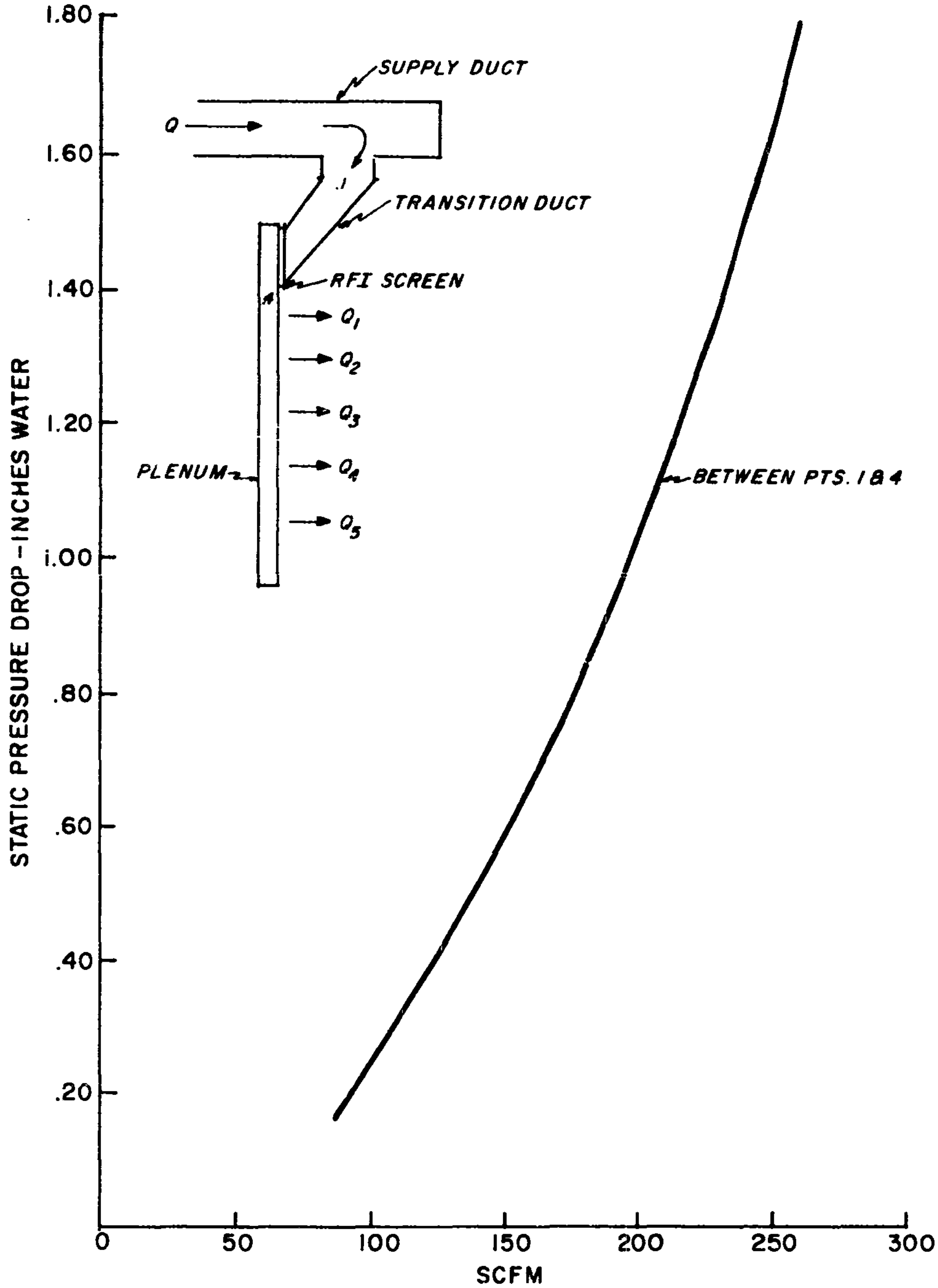


Figure 4-26. Pressure drop vs CFM for rack ducting - condition 2.

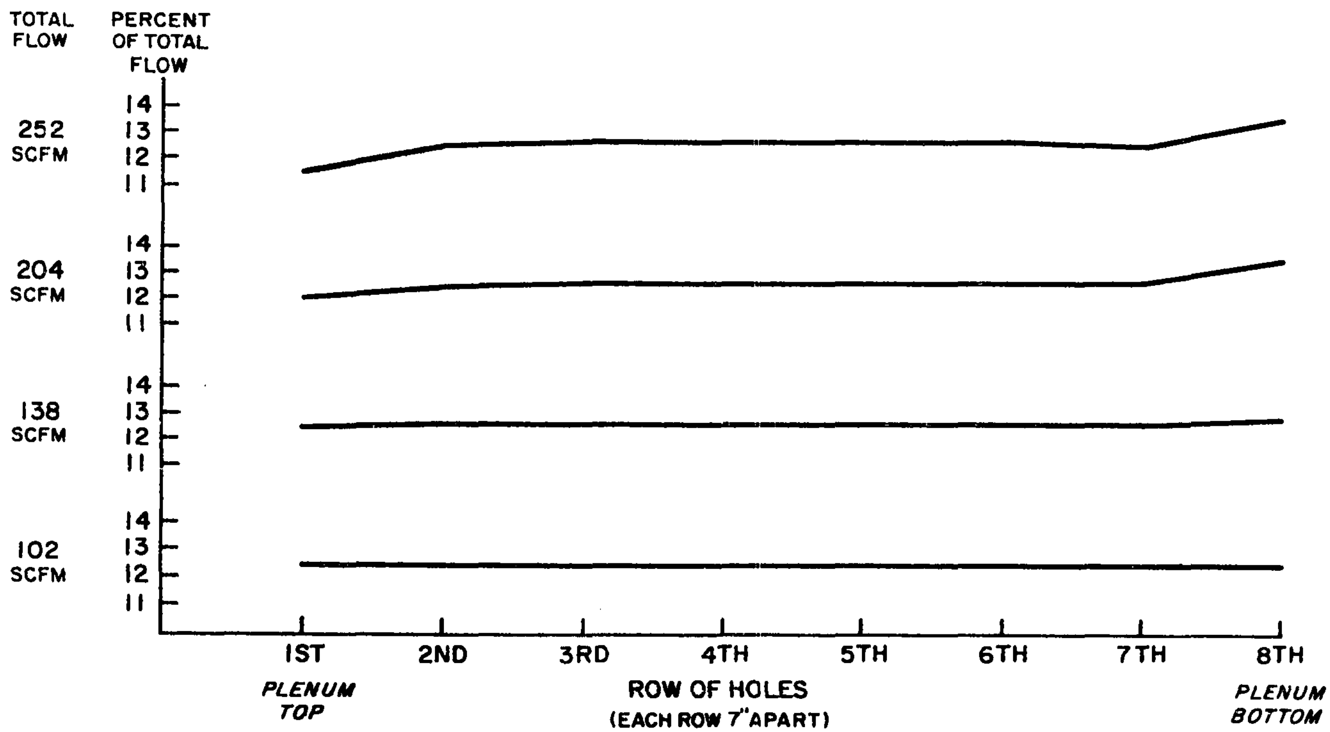


Figure 2-27. Variation of flow through orifice holes along plenum length.

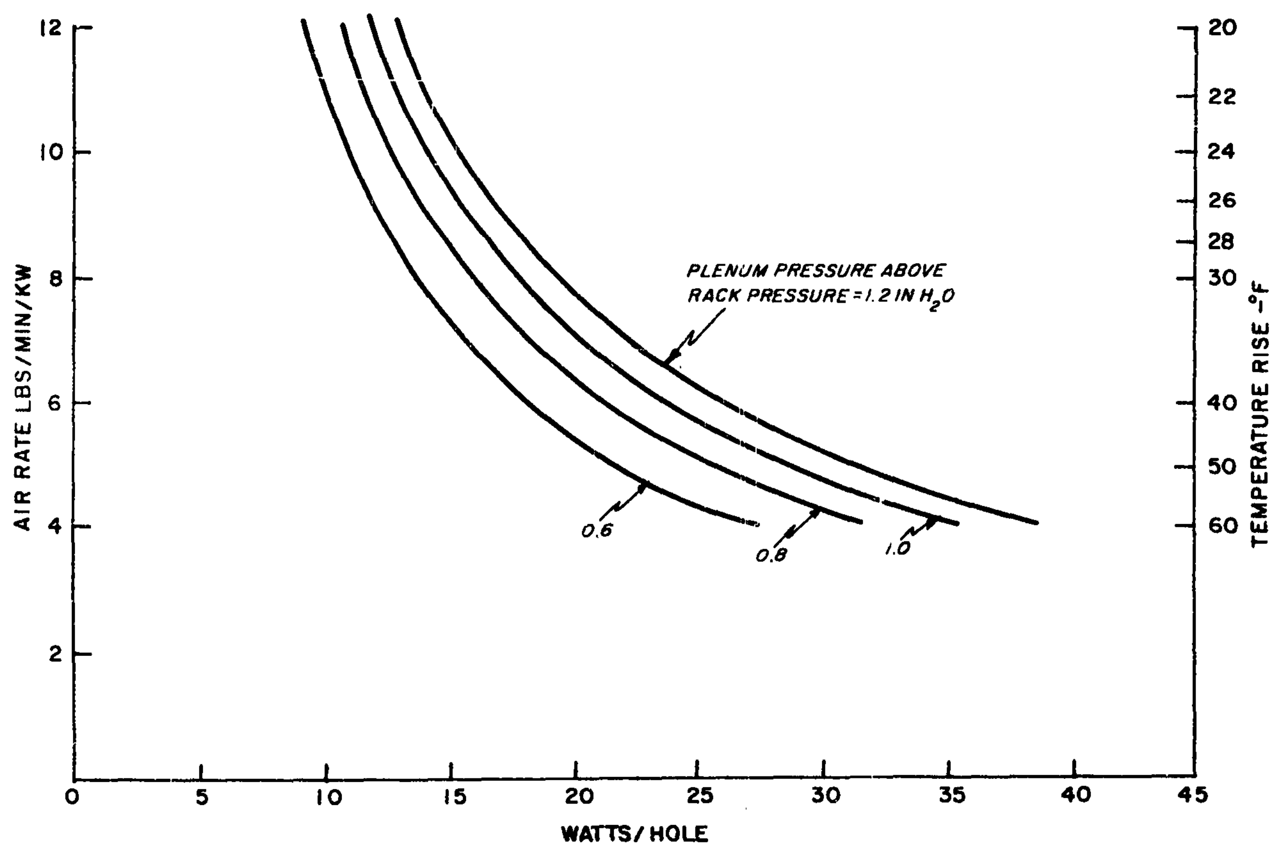


Figure 4-28. Cooling capacity of 0.375 - diameter hole.

SECTION 5

SHELTER DESIGN AND LAYOUT

5.1 SHELTER DESIGN

5.1.1 DESIGN OBJECTIVE

To house groups that compose a functional unit of MTE.

5.1.2 PROGRESS

Progress on the shelter design and layout effort is reported under the following headings:

(1) Shelter weight analysis
(2) Shelter intercabling
(3) Shelter rack interface
(4) Shelter shock and vibration
(5) Shelter handling

No significant changes have occurred in the following areas described in the previous Quarterly Interim Technical Report: General Equipment Arrangement and Configuration, Shelter Work Surfaces Definition, and Shelter Lighting.

5.1.3 SHELTER WEIGHT ANALYSIS (See Table 5-1 through 5-4)

The following tables summarize MTE weight estimates. Previous and present estimates are shown; it is seen that the total weights for ETG-1, ETG-2, and HTG have been decreased.

The changes in individual weight figures arose either as the result of reconfiguration of functions or as the result of more definitive information on the various items. Changes in weight which are of major significance are explained.

Table 5-1. ETG-1 weight tabulation

Item	Weight (pounds)			
	Previous		Present	
Shelter complement		2355		2485
Equipment complement				
Operator control console		919		890
Racks with equipment				
Measurements	501		460	
Computer/controller	514		488	
HF stimulus 1	487		498	
HF stimulus 2	474		533	
Tape transport	469		484	
Total		2445		2463
Storage cabinet		375		375
UUT liquid cooler		150		150
Tools		175		40
Work table and stool		50		50
Interrack wiring		250		250
TOTAL WEIGHT, ETG-1		6719		6703

Table 5-2. ETG-2 weight tabulation

Item	Weight (pounds)	
	Previous	Present
Shelter complement	2355	2485
Equipment complement		
Racks with equipment		
DC stimulus	853	558
Internal power supply 1	592	456
Internal power supply 2	487	413
Storage cabinet	375	375
LF stimulus 1	712	502
LF stimulus 2	610	640
Total	3629	2944
Interrack wiring	175	175
External cable assemblies	400	400
TOTAL WEIGHT, ETG-2	6559	6004

Table 5-3. Weight tabulation

Item	Weight (pounds)	
	Previous	Present
Shelter complement	2355	2485
Equipment complement		
Operator control console	746	679
Racks with equipment		
Control and stimulus	633	525
Internal power supply	445	365
Measurements	551	526
Total	1629	1416
Storage cabinet	440	220
Work bench and pneumatics	111	111
Tools	40	40
Hydraulic test stand	1100	1100
Oil	200	200
Pneumatic pump (swingout)	45	45
Interlock wiring	175	175
External cable assemblies	400	400
TOTAL WEIGHT, HTG	7241	6871

Table 5-4. Weight breakdowns of major subassemblies

Item	Weight (pounds)	
	Previous	Present
Shelter		
Shelter (basic)	1500	1500
Air conditioners (2)	360	360
Air conditioning ducts	120	120
Rack bases	200*	130*
Miscellaneous equipment	150**	350**
Lighting and service outlets	25	25
TOTAL WEIGHT, SHELTER	2355	2485
Electronic equipment rack		
Rack (basic)	95	95
Equipment mounting complement		
Air duct transition	0.6	0.6
Plenum	6.2	6.2
Connector panel frame	2.9	2.9
TOTAL WEIGHT, ELECTRONIC EQUIPMENT RACK	10.5	10.5
Level mounting complement		
Slide brackets	0.2	0.2
Slides (1 pair)	4.0	4.0
Connector panel	1.8	1.8
TOTAL WEIGHT, LEVEL MOUNTING COMPLEMENT	6.0	6.0

* 200 lb is pre-design estimate. 130 lb is present design.

** 150 lb is initial estimate. 350 lb includes estimate of 163 lb for addition of grounding straps, estimate of 70 lb for addition of air conditioner supports, and re-estimate of 117 lb for other miscellaneous equipment.

Table 5-4. Weight breakdowns of major subassemblies (cont)

Item	Weight (pounds)	
	Previous	Present
Storage cabinet		
Basic rack	95	95
Door and shelves	30	30
Load	250	250
TOTAL WEIGHT, STORAGE CABINET	375	375
Interrack wiring per rack	35	50
1/2 Storage cabinet		
Cabinet	70	70
Load	150	150
TOTAL WEIGHT, 1/2 STORAGE CABINET	220	220
Hydraulic - pneumatic control console		
Console	290	220
Intrarrack wiring	60	60
TOTAL WEIGHT, HYD-PNEU CONTROL CONSOLE	350	280
Electronic control console		
Console	320	220
Intrarack wiring	75	94
TOTAL WEIGHT, ELECTRONIC CONTROL CONSOLE	395	314
UUT liquid cooler		
Cooler, cabinet, and work surface	150	150

Table 5-4. Weight breakdowns of major subassemblies (cont).

Item	Weight (pounds)	
	Previous	Present
Work table and tools		
Surface and stool	50	50
Tools	100	100
Panel and light	25	25
TOTAL WEIGHT, WORK TABLE AND TOOLS	175	175
External cable assemblies		
Reel and tie downs	75	75
Cable assemblies	325	325
TOTAL WEIGHT, EXTERNAL CABLE ASSEMBLIES	400	400
Workbench and pneumatics (HTG)		
Work bench and storage cabinet	75	75
Compressor control	10	10
Accumulator	26	26
TOTAL WEIGHT, WORKBENCH AND PNEUMATICS	111	111

5.1.4 SHELTER INTERCABLING

The original concepts on shelter intercabling were presented in the Second Quarterly Interim Technical Report. Three major types of cabling were considered: primary power, intershelter signal cabling, and external UUT cabling. As shown in Figure 5-1, a single cable entry panel will be required for the primary power and intershelter cabling. A preliminary wire count is shown in Figures 5-2 through 5-4. Space has been allocated for growth or modification.

External UUT cabling is necessary for test of large UUTs which cannot be brought into the shlter for test. At AMICOM direction, no external cabling will be designed for the Development Model MTE, although entry panels will be provided to add external cabling at such time as the requirement can be fully defined.

5.1.5 SHELTER-RACK INTERFACE

A shelter-rack interface (Figure 5-5) has been developed to ensure compatibility of the shelter mounted equipment. The top mounting brackets from rack to shelter wall are subject to modification pending outcome of shelter shock and vibration environmental tests.

5.1.6 SHELTER SHOCK AND VIBRATION

The environmental design conditions are described in "Environmental Requirements Study Report (CR-62-547-8)' dated 21 June 1962 and specification MTE 5710.[1] The qualification tests are described in Specification MTE 5710.

In line with the environmental design conditions and the test requirements, the following criteria will be used for the shelter vibration-and-shock isolation devices:

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(1) This specification is included as Appendix A

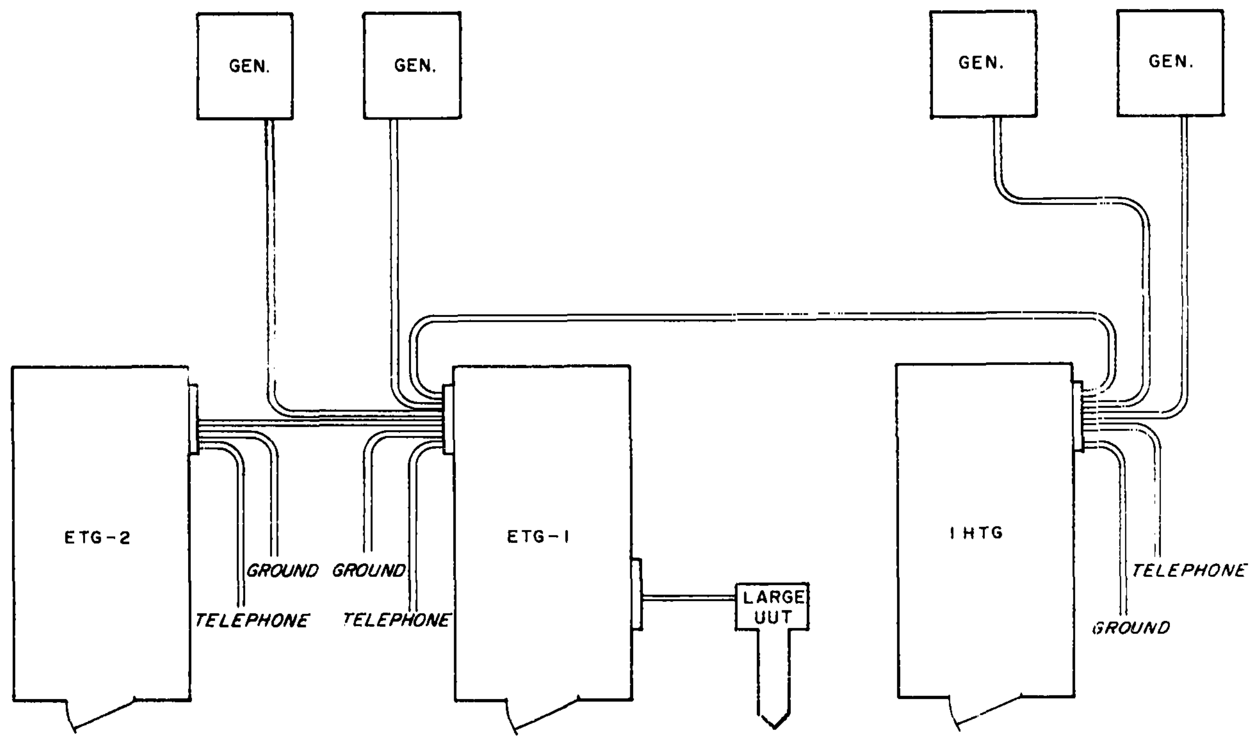


Figure 5-1. Intershelter cabling.

TYPE SIGNAL	CONNECTING TO OR FROM		NO. OF WIRES REQ'D	WIRE SIZE	QTY OF PINS/CONN.	QTY OF CONN. REQ'D
A-C PRIM POWER	—	ETG-I	8	#0	4	2
DC POWER	ETG-I	--	24	#16	21	2
PROGRAM	—	ETG-I	60	#22	55	2
L F STIM COAX	ETG-I	....	20		7	3
L F STIM	ETG-I	—	70	#20	36	2
D-C STIM	ETG-I	—	30			3
D-C RETURN	ETG-I	—	2	#0	2	1
GROUND						1
TELEPH.						1

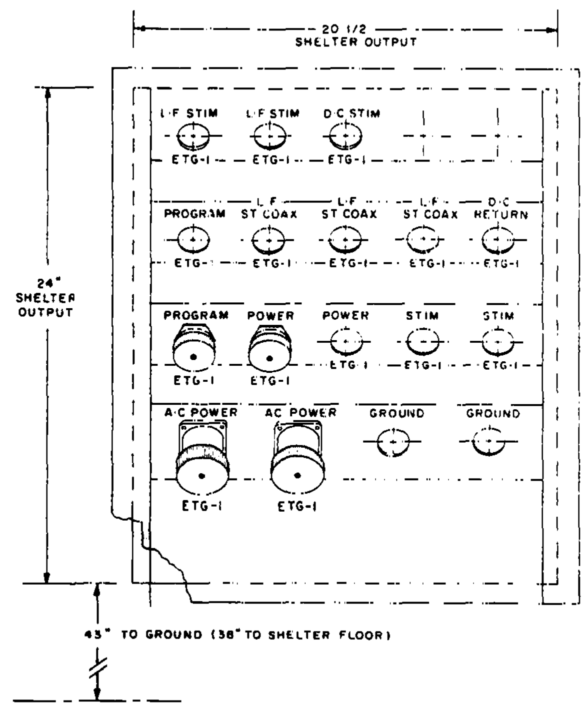


Figure 5-2. ETG-1 cable entry panel

TYPE OF SIGNAL	CONNECTING TO OR FROM		NO. OF WIRES REQ'D	WIRE SIZE	QTY OF PINS/CONN.	QTY OF CONN. REQ'D
A-C PRIM. POWER		GEM	8	0#	4	2
A-C PRIM. POWER	ETG-2		8	0#	4	2
DC POWER		ETG-2	24	#16	21	2
PROGRAM	ETG-2		60	#22	55	2
PROGRAM	HTG		60	#22	55	2
L-F STIM COAX		ETG-2	20	#8	7	3
L-F STIM		ETG-2	70	#20	36	2
D-C STIM		ETG-2	30	#8 #6	10 20	3
D-C RETURN		ETG-2	2	#0	2	1
GROUND						1
TELEPH						1

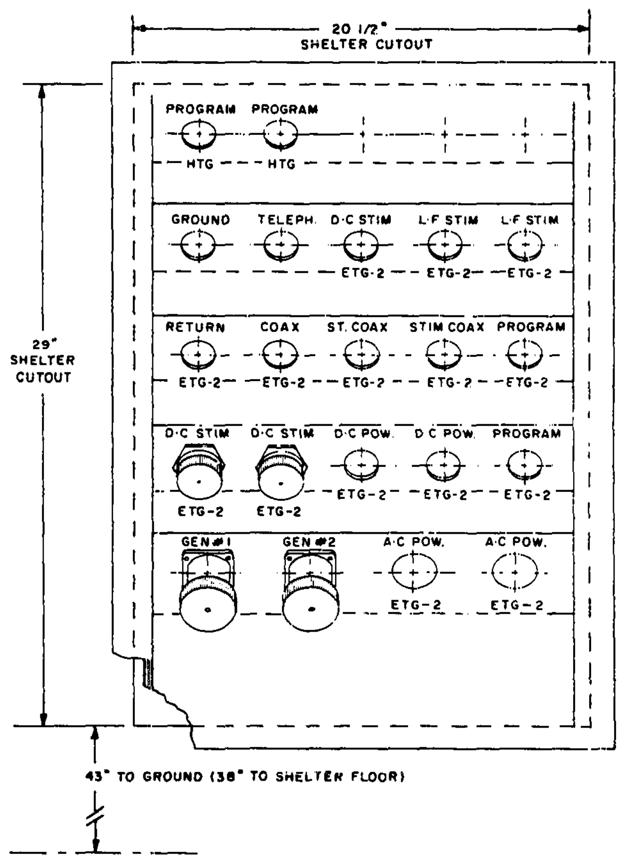


Figure 5-3. ETG-2 cable entry panel

TYPE OF SIGNAL	CONNECTING TO OR FROM		NO OF WIRES REQ'D	WIRE SIZE	QTY OF PINS/CONN.	QTY OF CONN. REQD
A.C. PRIM POWER	—	GEN	8	#0	4	2
PROGRAM	ETG-I	—	60	#22	55	2
GROUND						I
TELEPH.						I

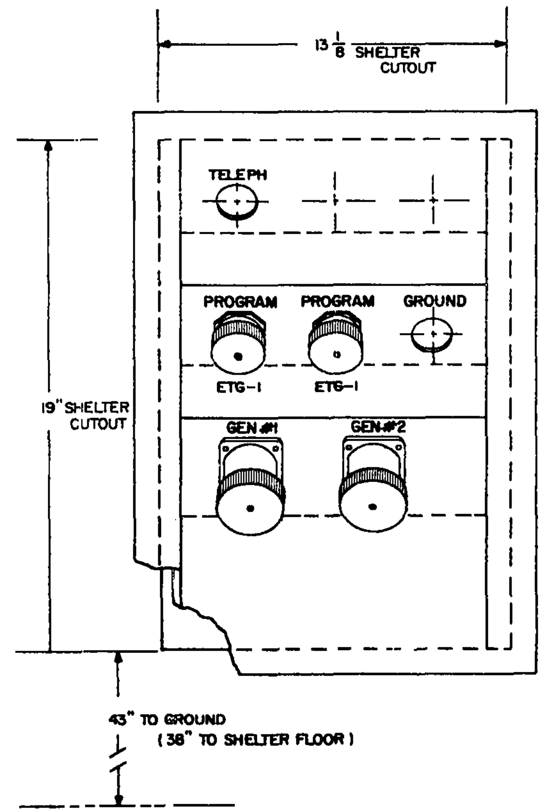


Figure 5-4. HTG cable entry panel

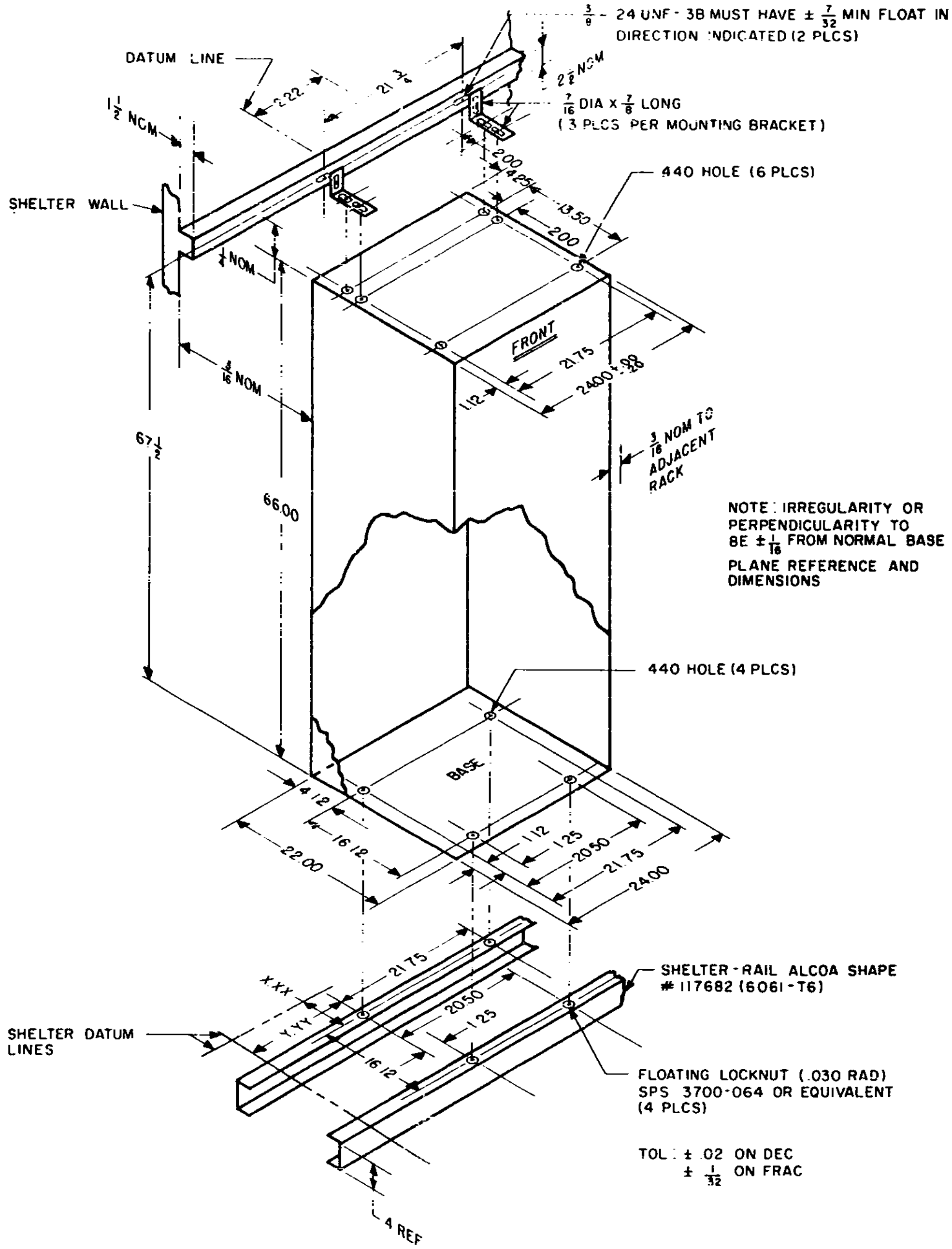


Figure 5-5. MTE shelter - rack mounting interface

The shelter shock devices will be designed to transmit to the shelter equipment shock load not exceeding 10g when subjected to the following conditions:

20 g vertical,	11 millisecond duration
20 g longitudinal,	11 millisecond duration
10 g lateral,	11 millisecond duration

This will permit hard un-isolated mounting of the racks, chassis and consoles inside the shelter. The desirability of hard mounting has been demonstrated at the Aberdeen Proving Ground and, most recently, by the 4000-mile endurance tests for the Pershing firing units. In addition to the environmental design conditions, the shelter shock devices (or skids) are to be specified and tested to the parameters of MIL-S-52059A with the following exception: the drop test height specified will be 12 inches instead of 18 inches.

MTE specification 5707[2] will be revised to clearly discribe the above requirements and test conditions.

During the next quarter the shelter specification MTE 5707 for procurement of the developmental model will be revised and released.

5.1.7 SHELTER HANDLING

A limited anaylsis was completed covering the possible use of the Telefork 102, with boom attachment for loading and unloading an MTE Shelter unit on the M-55 truck. Data was obtained from USAMOCOM, Natick, Mass.

Dimensional data was limited to assembly drawings of the basic Telefork 102, actual photographs of the unit with boom attached, and as layout of the boom assembly. Subsequent composites of this information are subject to scaling inaccuracies.

(2) This specification is included as Appendix B.

The resulting sketch (see Figure 5-6) depicting this application with the boom in the maximum lift position indicates an approximate lifting clearance of two feet and adequate lateral clearance assuming a maximum sling offset to accommodate large variations in shelter center of gravity.

5.2 SHELTER AND EQUIPMENT MOCKUPS

Construction of full-scale mockups of Electronic Test Group No. 2 and Hydraulic Test Group was begun and was carried to the point where the mockups of the basic shelters, with air conditioning units, and ducts were completed, and mockups of all racks, consoles, and work areas were completed, except for the front panels.

During the next quarter the front panel mockups for ETG 2 and the HTG will be prepared. The mockup equipment will be installed in the shelters, thus completing the ETG 2 and HTG mockups.

5.3 HEATING, COOLING, AND VENTILATING DESIGN

The air-distribution elements are schematically illustrated in Figure 5-7.

In this closed-loop pressurized distribution system, it is seen that the conditioned air must be forced through each equipment rack at the same pressure drop, since the racks are a parallel circuit. The flow resistance of all the parallel paths must, therefore be the same. This value of flow resistance is defined by the rack having the highest thermal load. The flow resistances of the other parallel paths are then made the same by inserting orifices, so that each path will maintain its rated air flow at an identical pressure drop.

To obtain the total pressure required to force the necessary quantity of air through the system, the total system loss must be determined. This system loss can be categorized into the following pressure drops:

(1) The pressure drop from point S to point N,
(2) The pressure drop of the parallel paths (a typical one is from point N to point F.),
(3) The pressure drop from point F to point A.

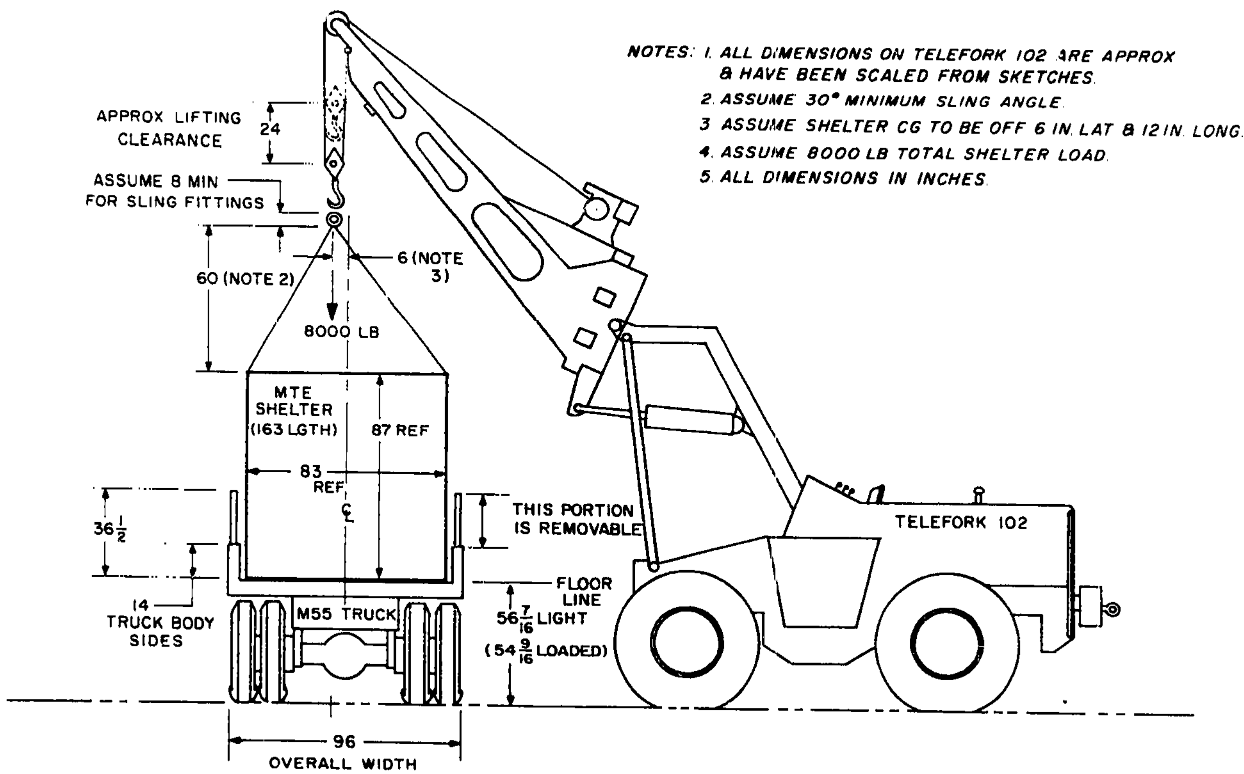


Figure 5-6. MTE shelter handling using Telefork 102

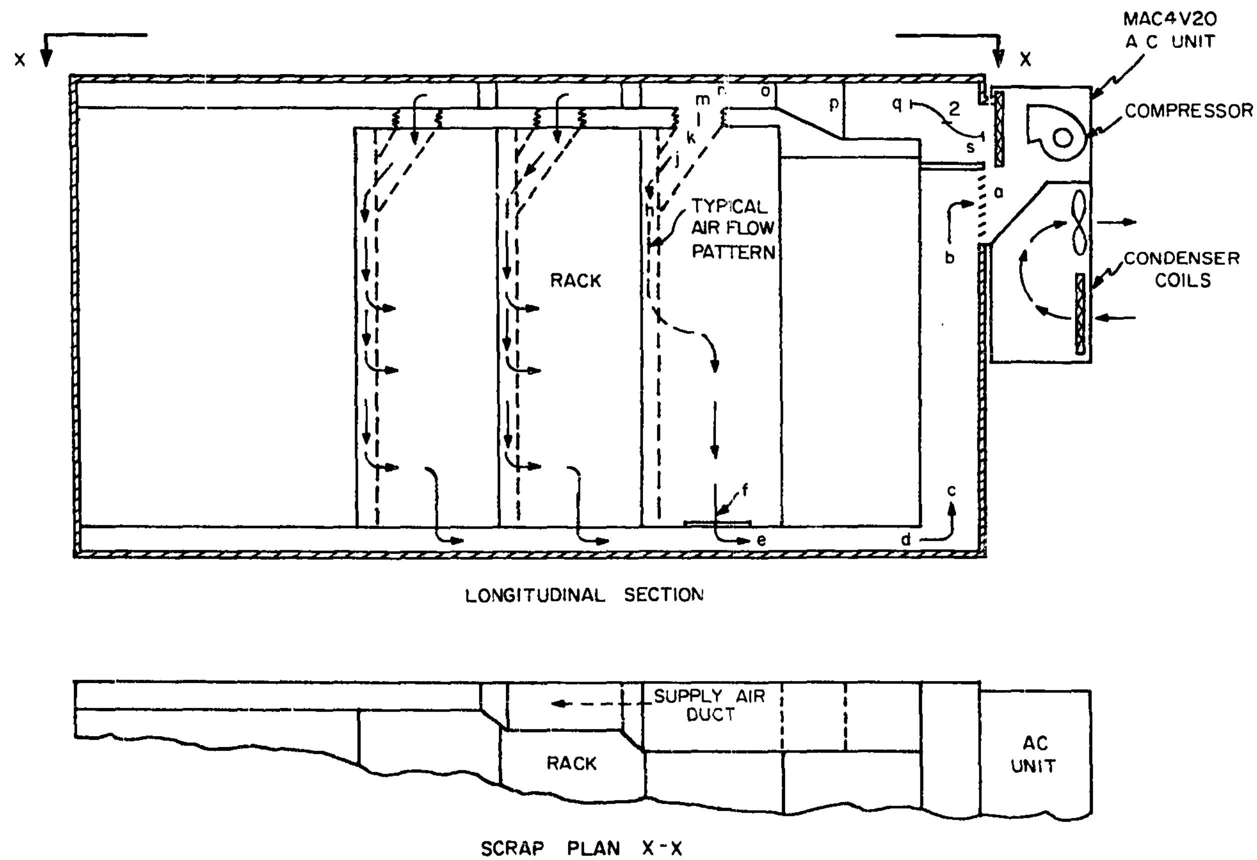


Figure 5-7. Air distribution paths

The maximum free-flow efficiency of the air conditioner is 640 CFM. A determination of the pressure drops will then permit an evaluation of booster-fan requirements.

At this time, however, detailed information on the thermal load of each parallel path is not available in final form. In the meantime, curves have been developed for other portions of the air distribution system and for typical orifices to permit a preliminary evaluation of the system at estimated thermal loads.

5.3.1 PRESSURE DROPS OF INTAKE AND EXHAUST DUCTS

The path from the air conditioner to the tops of the racks is shown in Figure 5-7 as s-r-q-p-o-n. The region between points r-q-p is an enlarged duct region reserved to accomodate the booster fan. The path from the bottoms of the racks to the exhaust is shown in Figure 5-7 as f-e-d-c-b-a. The curves shown in Figures 5-8 and 5-9 permit an evaluation of the pressure required to force various rates of air flow.

Tables 5-4 and 5-6 illustrate a typical calculation performed in the plotting of Figures 5-8 and 5-9, respectively. Total pressure at any point in the duct is composed of (1) velocity pressure and (2) static pressure. Friction losses are non-recoverable and are summed up for the paths indicated. Static pressures are assumed to be zero at the termination of the path.

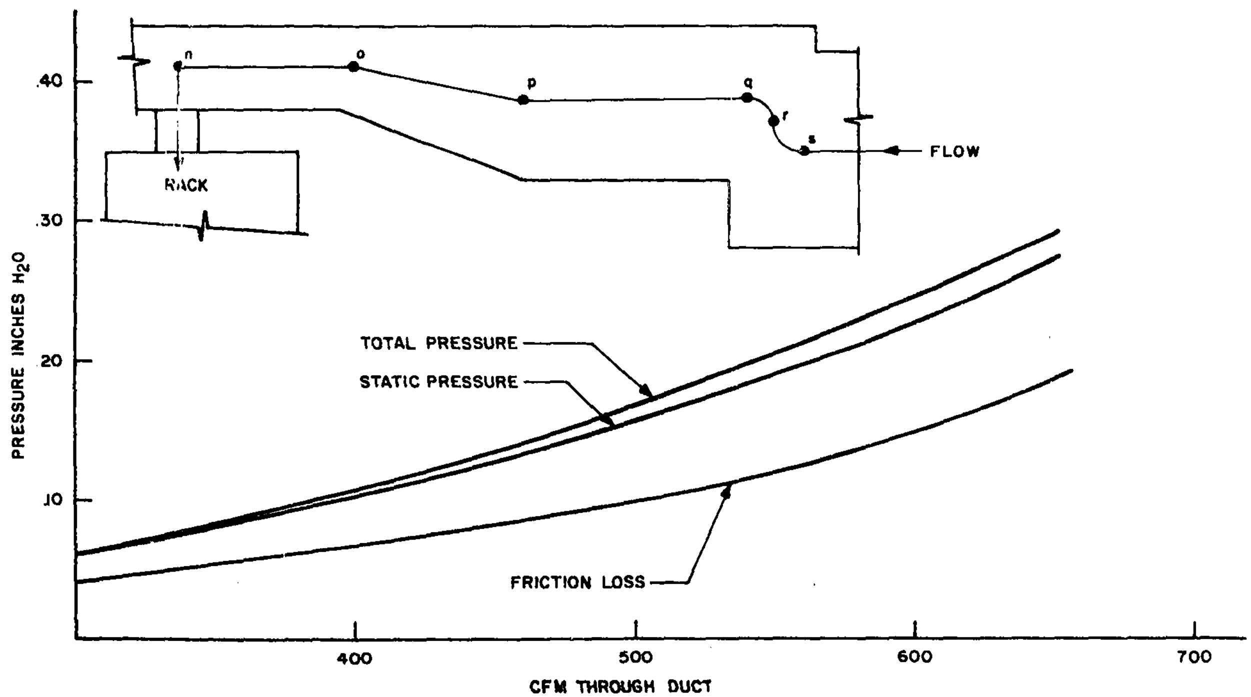


Figure 5-8. Pressure versus air flow draracteristics for path n-o-p-q-r-s

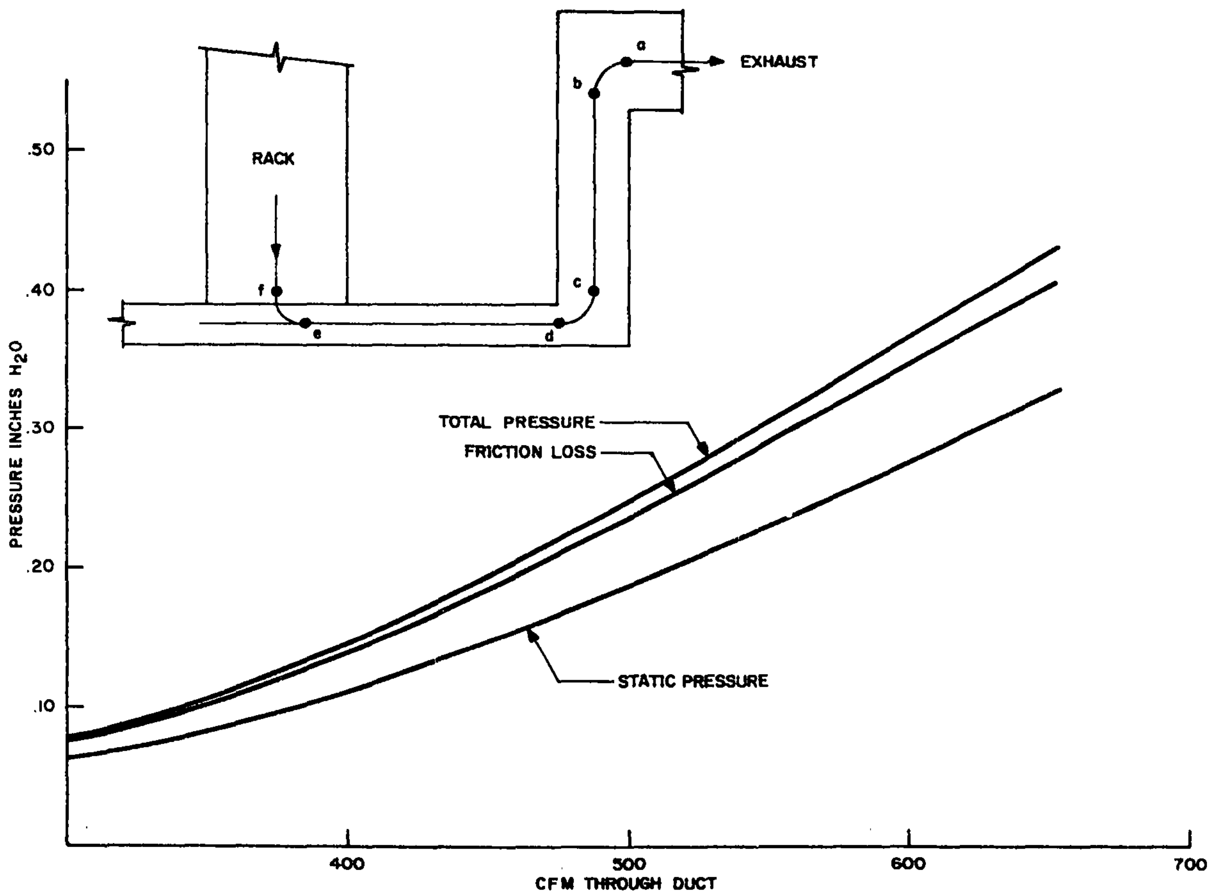


Figure 5-9. Pressure versus air flow for path a-b-c-d-e-f

Table 5-5. Typical summation of pressures for path s to n

Components of pressure	Pressures in inches of H_2O for 640 CFM air flow at points					
	n	o	p	g	r	s
Velocity pressure	0. 102	0. 102	0. 037	0. 037	0. 330	0. 016
Static pressure	0. 000	0. 007	0. 074	0. 076	0. 109	0. 261
Friction loss	0. 175	0. 168	0. 166	0. 164	0. 056	0. 000
Total	0. 277	0. 277	0. 277	0. 277	0. 277	0. 277

Table 5-6. Typical summation of pressures for path f to a

Components of pressure	Pressures in inches of H_2O for 640 CFM air flow at points					
	a	b	c	d	e	f
Velocity pressure	0. 011	0. 102	0. 102	0. 102	0. 102	0. 090
Static pressure	0. 000	0. 035	0. 043	0. 169	0. 175	0. 312
Friction loss	0. 391	0. 265	0. 257	0. 131	0. 125	0. 000
Total	0. 402	0. 402	0. 402	0. 402	0. 402	0. 402

5.3.3 ADJUSTMENT OF RACK PRESSURE DROPS

Curves have been developed (see Figure 5-10) showing ideal parameters for typical throttling orifices in the 4.5 - inch duct at the entraces to the racks. By use of these curves, orifices could be selected to make the flow resistance of each parallel path the same.

5.3.4 EVALUATION OF RESULTS AND PLANS

Evaluation of the air distribution system with the aid of the curves for estimated thermal loads implies that continued work with this distribution system may lead to a high - pressure air-distribution system with large penalties for

(1) specialized boost fans,
(2) increased space requirements,
(3) prime power increases with inherent increase of thermal load
(4) high noise levels
(5) limited flexibility of
 (a) thermal load variations,
 (b) equipment position, size, and orientation

These penalties are contrary to the basic philosophy of the MTE system concerning

(1) configuration and system flexibility,
(2) standardized design,
(3) minimization of equipment power and weight.

An alternate approach, eliminating the high-pressure requirements, boost fans, and pressure ducting will be investigated in the next period. This approach will utilize the shelter itself as a low-pressure distribution system, with individual low-pressure fans on racks and other thermal loads.

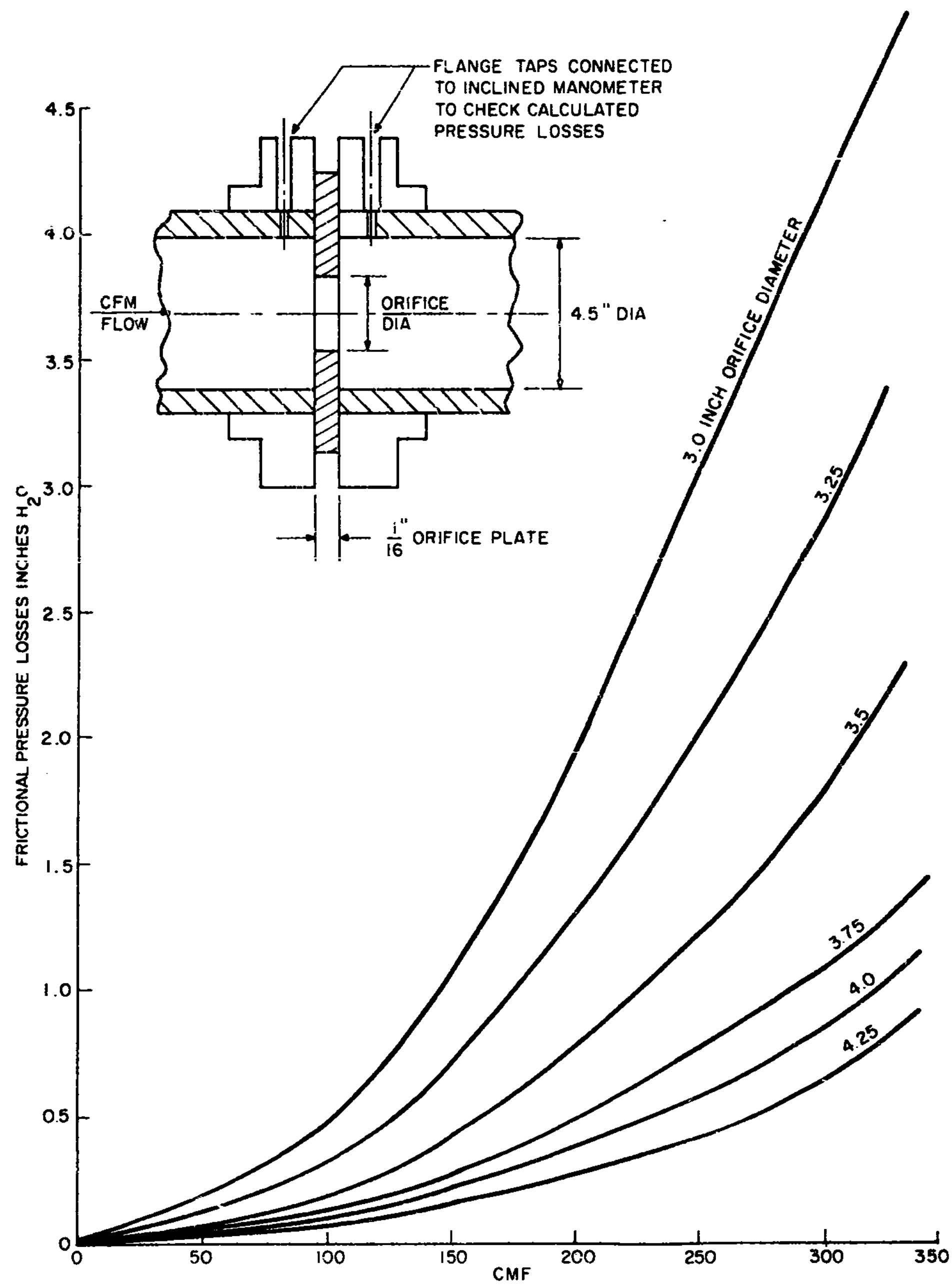


Figure 5-10. Frictional pressure losses through orifices in 4.5-inch-diameter duct.

SECTION 6

EQUIPMENT DEVELOPMENT

6.1 ELECTRONIC TEST SET

6.1.1 INTRODUCTION

Progress on equipment development during this quarter is reported under the following headings:

- Computer/Controller
- HF Stimulus
- LF Stimulus
- DC Stimulus
- Measurements
- Internal Power Supplies.

6.1.2 COMPUTER/CONTROLLER

A. <u>Equipment Division</u>

The Computer/Controller equipment has been divided into four sub-groups as shown in Figure 6-1:

- Computer equipment
- Controller equipment
- Peripheral equipment
- Display and control equipment.

A revised functional description of the assemblies in the Computer/Controller is contained in Appendix C.

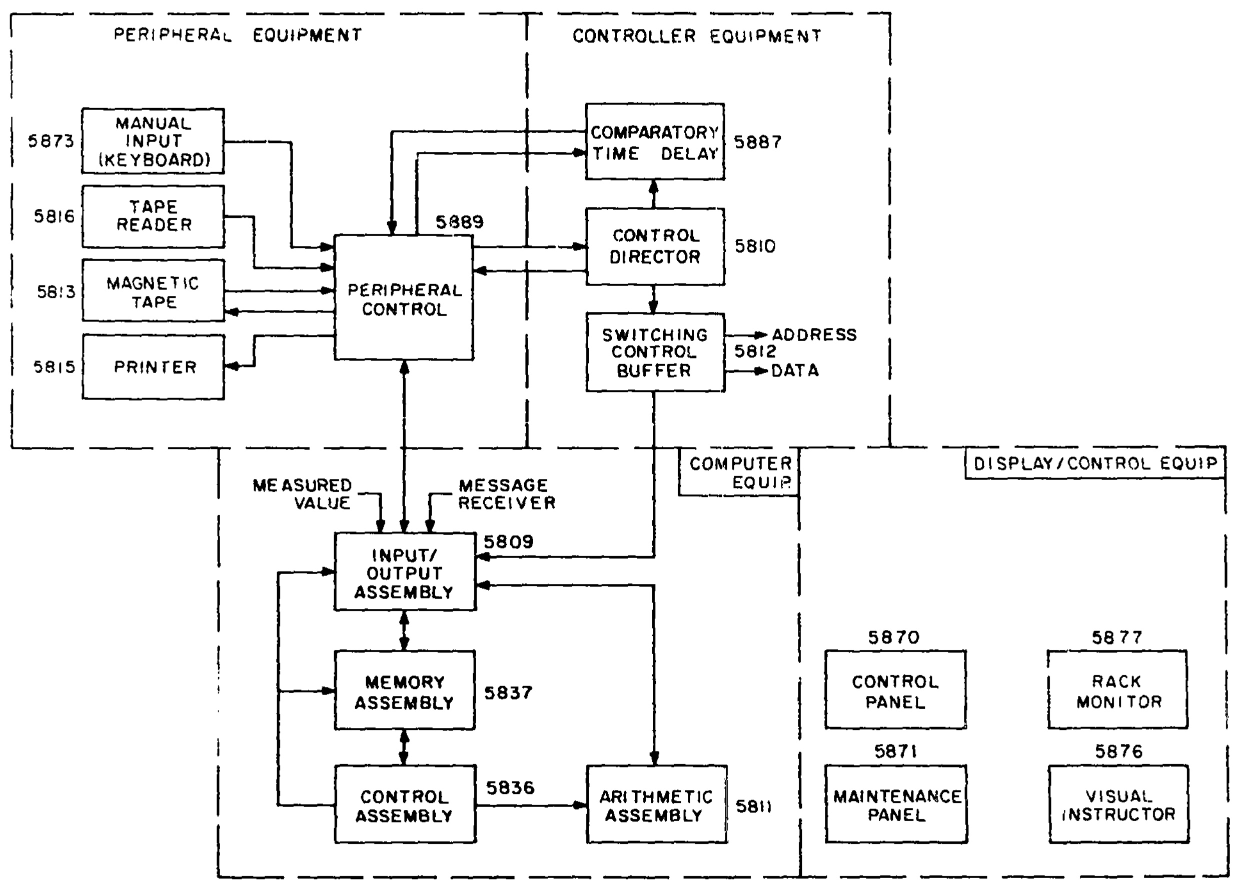


Figure 6-1. MTE Computer/Controller block diagram

B. Computer Equipment

1. Summary

The logical design of the computer equipment was completed during the quarter. All printed circuit boards (with the exception of those in the Control Assembly) were released to production.

2. Input/Output Assembly

a. Progress and Status

The performance specification for this assembly has been completed. The assembly consists of one chassis with twenty-two boards of five types. Both layout and photomasters of the five boards have been completed; board and chassis assembly drawings are in process.

b. Plans

(1) Conduct a design review of the Input/Output Assembly.

(2) Release the assembly to production.

3. Arithmetic Assembly

a. Progress and Status

The performance specification and logical design of this assembly have been completed. The logical design was accomplished in a fashion such that the whole assembly has been implemented with twenty-four identical boards. The photomaster for this board is complete; assembly drawings are in process.

b. Plans

(1) Conduct a design review of the Arithmetic Assembly.

(2) Release the assembly to production.

4. Control Assembly

a. Progress and Status

The performance specification and logical design of the Control Assembly have been completed. Transferral of the logic to printed circuit boards is proceeding.

b. Plans

(1) Conduct a design review of this assembly.
(2) Release the assembly to production.

5. Memory Assembly

a. Progress and Status

The performance specification and logical design of the Memory Assembly have been completed.

The core used in the memory stack has been changed from an RCA type 233M1 to an RCA type 0066M5, this results in reduced current demand on the driving circuits. The Program counter, formerly located in the Memory Logic Assembly, is now located in the Memory Assembly resulting in fewer leads between chassis. The Memory Logic Assembly is now part of the Input/Output Assembly, again resulting in fewer leads between chassis.

The decoders and X-Y drivers have been designed and preliminary board layouts are complete. The Read-Write switches and inhibit drivers have been designed, both utilizing the same circuit. The timing circuitry and sense amplifiers have been designed and are undergoing environmental test. Design of the Program Counter is complete and is undergoing board layout. The Memory Stack has been ordered, the diode boards have been released to production, and the resistor and capacitor boards are undergoing layout.

b. Plans

(1) Conduct a design review of the Memory Assembly.

(2) Release the assembly to production.

C. Controller Equipment

1. Summary

The logical design of the Controller reached approximately 70% completion during the quarter. The logical design of the millimodule boards for two of the three Controller assemblies was completed; layout of these boards has been started. The release of all long-lead items was completed; millimodule types and quantities have also been released.

2. Control Director

a. Progress and Status

The interface definition between the Control Director and the Computer reached 50% completion; logical design of the unit reached approximately 25% completion.

b. Plans

(1) Complete the interface definition with the Computer and peripheral equipments.

(2) Complete the logic design of the unit.

(3) Complete board layouts, and release to production.

(4) Complete to-from wiring list.

(5) Start preparation of test specifications and test procedures.

3. Switching Control Buffer

a. Progress and Status

During this quarter the interrelationship of the Switching Control Buffer with the following groups was defined: HF Stimulus, LF Stimulus, DC

Stimulus, Measurement and Time Interval and Frequency Meter. The detailed interrelationships for one of these groups is described in Appendix D.

The logical design of the millimodule boards for this unit is complete; Table 6-1 shows the quantities, types, and status of the required boards.

Table 6-1. Millimodule boards for switching control buffer

Board Type	Quantity	Logic Design - Percentage Complete
3 BCD Storage*	4	100
Line Driver - I*	6	100
Line Driver - NI*	1	100
Address Verify	2	100
Binary Decoder	4	100
3 Input Power NAND	6	100
Switching Control A	2	100
Switching Control B	1	100

* Standard MTE Millimodule Boards

b. Plans

(1) Complete board layouts and release to production.

(2) Complete to-from wiring list.

(3) Start preparation of test specifications and test procedures.

4. Comparator/ Time Delay

a. Progress and Status

The logical design of this unit was reported complete in the last Quarterly Report; Appendix E contains a detailed functional description of the unit. During this quarter the logical design of the millimodule boards was completed; Table 6-2 shows the quantities, types, and status of the required boards.

Table 6-2. Millimodule boards for comparator/ time delay unit

Board Type	Quantity	Logical Design - Percentage Complete
Digital Comparator	1	100
Comparator Logic	1	100
Tape Search Logic	1	100
Multiplexer	2	100
DAR Multiplexer	1	100
Line Driver - NI*	1	100
Decade Counter	2	100
Time Delay Control	1	100
3 BCD Storage*	1	100

* Standard MTE Millimodule Boards

b. Plans

(1) Complete board layouts and release to production.

(2) Complete to-from wiring list.

(3) Start preparation of test specifications and test procedures.

D. Peripheral Equipment

1. Status and Progress

During this quarter RCA recommended vendors for all items of peripheral equipment: the Tape Reader, Printer, Magnetic Tape Transport and Manual Input. The Tape Punch was eliminated from the system by TDO-20. The Printer, a militarized unit manufactured by Potter Instruments Company, and the Tape Reader, a militarized unit manufactured by Photocircuits Corporation, were authorized by TDO's 25 and 27. Approval has not yet been received for the Magnetic Tape Transport, a militarized cartridge type unit manufactured by the Surface Communications Division of RCA, and for the Manual Input, a militarized and completely modularized unit manufactured by Soroban.

The control function equipment required by each of the items of peripheral equipment (but not included within each such equipment) requires only a small volume. These control functions, therefore, have been combined into a single unit, the Peripheral Control Assembly. Logical design of this unit is nearing completion; a preliminary block diagram of the unit is shown in Figure 6-2.

2. Plans

(a) The design of the Peripheral Control Assembly will be completed and the unit will be released for production.

(b) Upon approval, the remaining items of peripheral equipment will be released for procurement. Liaison will be maintained with the vendors of all items of peripheral equipment.

(c) Development of test plans and test procedures will be started.

E. Display/Control Equipment

1. Status and Progress

The display/Control Equipment consists of the Control Panels, Maintenance Panel, System Status Monitors and Visual Instructor.

The functions of these units were extensively reviewed and revised during the quarter to achieve the operations required by the MTE system. Layouts have been finalized and circuits are being designed.

2. Plans

(a) Conduct a design review.

(b) Review the panel designs with AMCOM.

(c) Release the Control and Display equipment to production.

6.1.3 HIGH FREQUENCY STIMULUS

The simplified block diagram for the High Frequency Stimulus is given in Figure 6-3. Progress on each of the fourteen assemblies is reported individually in the following paragraphs.

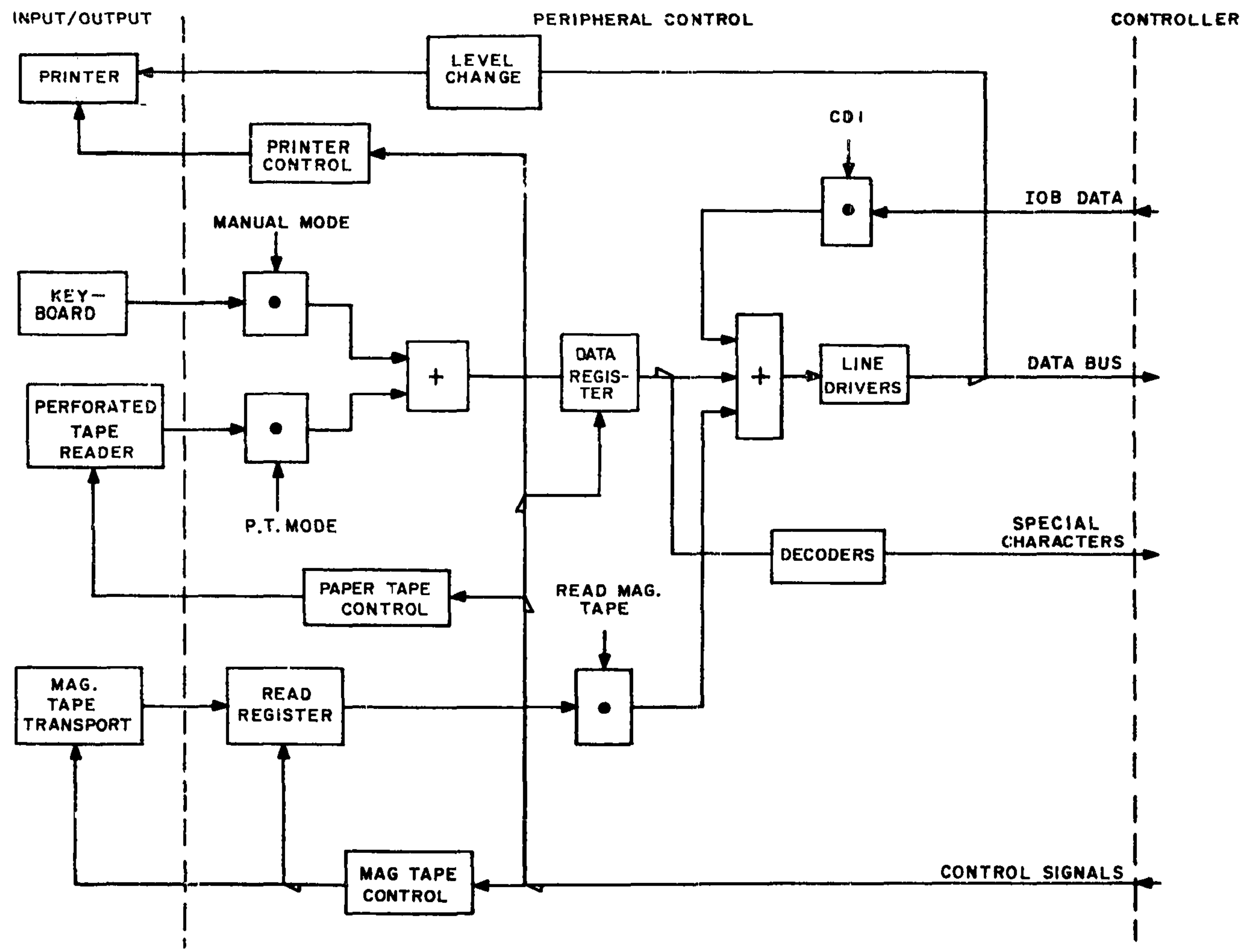


Figure 6-2. Simplified block diagram peripheral control assembly

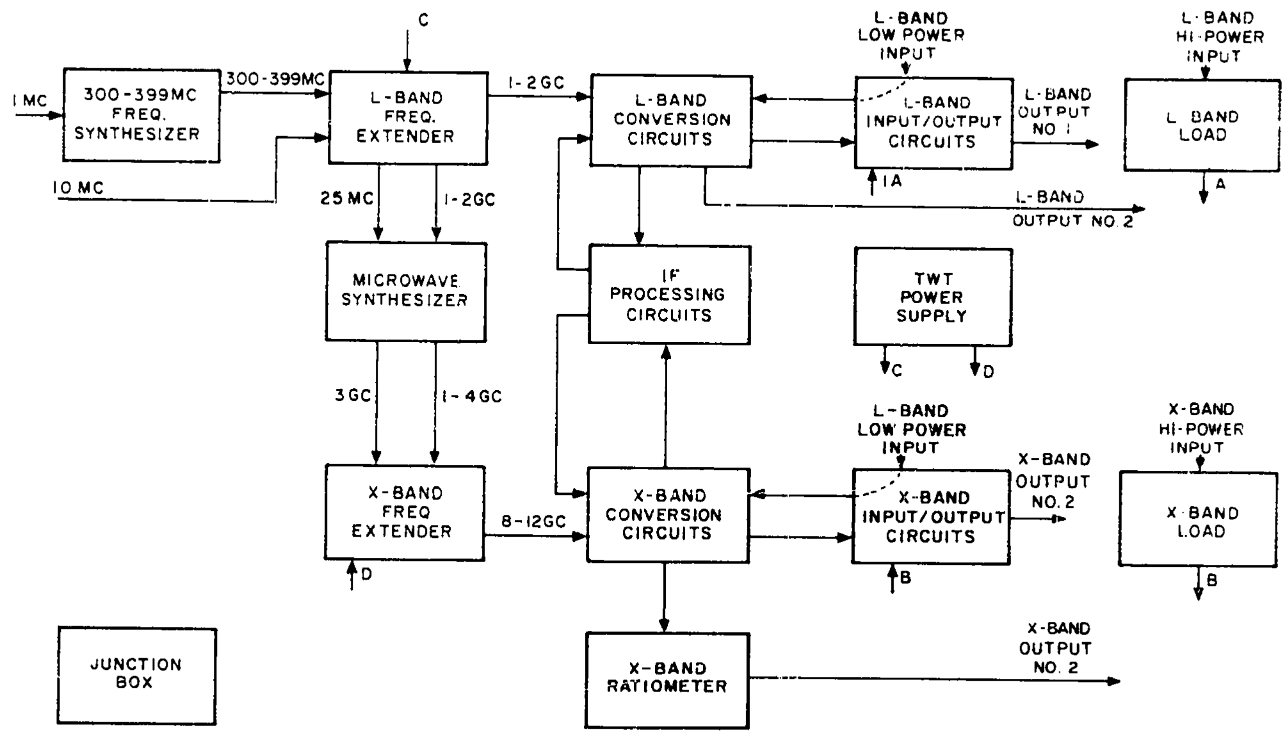


Figure 6-3. High frequency stimulus - simplified block diagram

A. 300-399 Mc Frequency Synthesizer

a. Progress and Status

Integration of the Frequency Synthesizer circuits was accomplished. See Figure 6-4. Spot checks at several points across the band (315-320 Mc, 347-349 Mc, 370-375 Mc) showed successful locking.

The 28-37 Mc and 20-29 Mc interpolator loops perform reliably with spurious content down 40 db or more. The X10 multiplier and filter operate satisfactorily and unwanted frequencies are down to a level of insignificance (-30 db), because the high frequency phase detector loop will only respond to a strong correction frequency no more than 2.5 Mc away from the mixer output carrier in an overall passband of 18-30 Mc.

Spurious outputs at a typically locked carrier of 348 Mc are better than 35 db down from the carrier. These spurious outputs are 1 Mc sidebands which find their origin in the pulse locked oscillator. Some sidebands exist in the 20-29 Mc phase lock loop as spectral lines from the 20-29 Mc interpolator oscillator. Test and level corrections will continue during the next quarter to ensure that the unwanted products are below -40 db throughout the band from 300-399 Mc.

Because of a decrease in correction voltage sensitivity of the 300-399 Mc oscillator at the high end, it will be necessary to modify the present frequency error discriminator circuitry to

(1) provide an error voltage capable of locking at high frequencies from an offset of 2 Mc plus drift either way from the programmed carrier, and
(2) provide similar locking at the lower frequencies without causing instability because of the increased loop gain.

The digital to analog conversion circuits and the 100 volt regulator circuit have been finalized and laid out on printed boards. The original program voltage

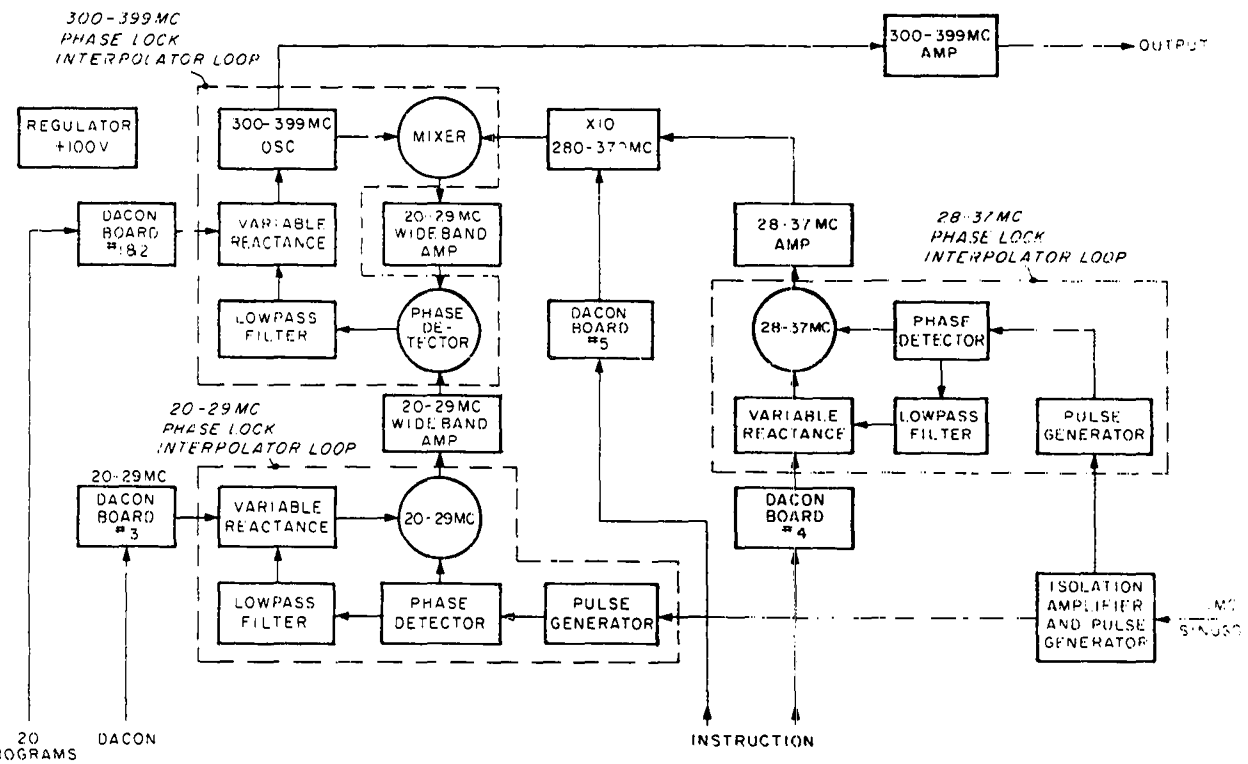


Figure 6-4. 300-399 Mc frequency synthesizer - block diagram

supply has been changed from 120V to 100V to improve reliability of the DACON circuits.

The 300-399 Mc Frequency Synthesizer was released to manufacturing, but some changes are anticipated in the frequency error discriminator.

b. Plans

During the next quarter, breadboard effort will continue on the 20-29 Mc loop and on the 300-399 Mc error discriminator circuits. The integrated breadboard will be subjected to temperature environmental testing.

B. L-Band Frequency Extender

A block diagram of the L-Band Frequency Extender is shown in Figure 6-5.

a. Multipliers

(1) Progress and Status

Design work on the multiplier chain was completed. A 5 Mc signal was made available from the Low Frequency Stimulus as input to the multipliers. This permitted simplification of the circuit by elimination of the divide-by-two circuit. Thus the assembly now consists of a X5 multiplier (consisting of a 5-Mc amplifier, transistor quintupler, 25-Mc filter, and power divider) followed by a varactor quadrupler.

The 100-Mc output of the quadrupler is amplified to the required 1-watt level. Tests on the new design are near completion.

(2) Plans

All evaluation of the breadboard assembly including these circuit changes will be completed and the design released to drafting and for manufacturing during the next quarter.

b. Cavity Harmonic Generators

(1) Progress and Status

A single harmonic generator with printed waveguide filters was found to be inadequate. The filters were lossy, hence a shift to cavities was indicated.

As suggested in the previous quarterly report a separate harmonic generator has been designed for each of the 10 desired frequencies. A series of charge storage diode harmonic generators employing lumped parameter circuit techniques at the fundamental input frequency of 100 Mc and distributed constant circuits at each of the UHF L-Band outputs has been designed. The cavities used as output harmonic tank circuits are of the foreshortened coaxial quarter-wavelength type. The foreshortening capacitance tunes the cavity over a range of 300 Mc to 400 Mc. Three models will therefore provide adequate coverage from 700 Mc to 1600 Mc. A breadboard unit of each of the three models has been built and tests are now in progress.

The couplings to the cavities are of the magnetic loop type. The inclusion of feed-through capacitors for grounding the loop allows the application of a self bias control voltage to enhance the efficiency of the input loop coupling and harmonic generation. For the output loop the feed-through provides a means of applying DC bias to the diode cluster used for frequency selection.

At the input to the cavity harmonic generators, the 100-Mc signal from the multipliers must be switched to the unit that is to give the desired output frequency. This is accomplished with a multiple pole coaxial switch controlled by BCD logic.

(2) Plans

During the next quarter tests on these new harmonic generator designs will be completed, and the generators will be released for manufacturing.

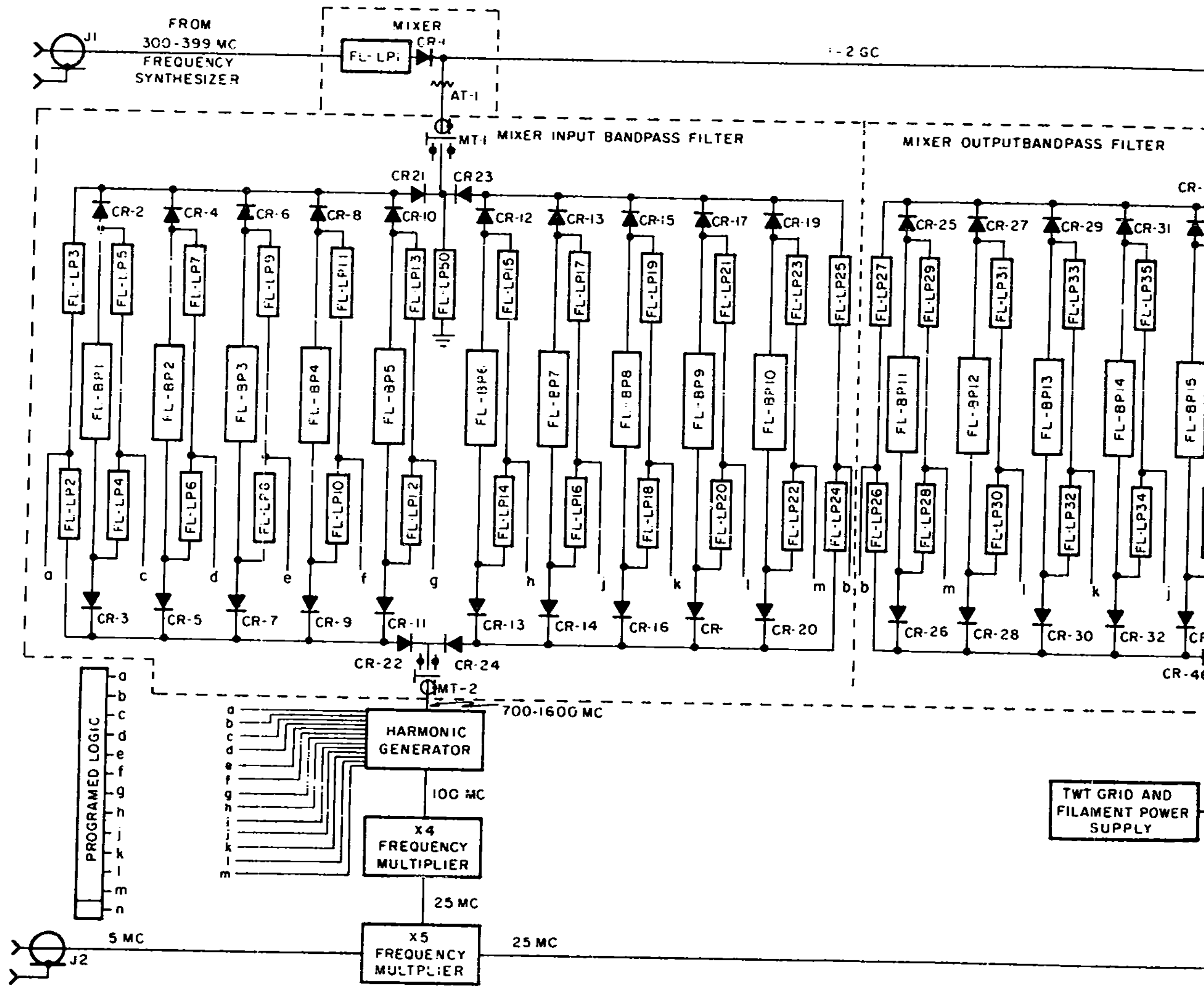


Figure 6-5. L-band frequency extender - block diagram

1

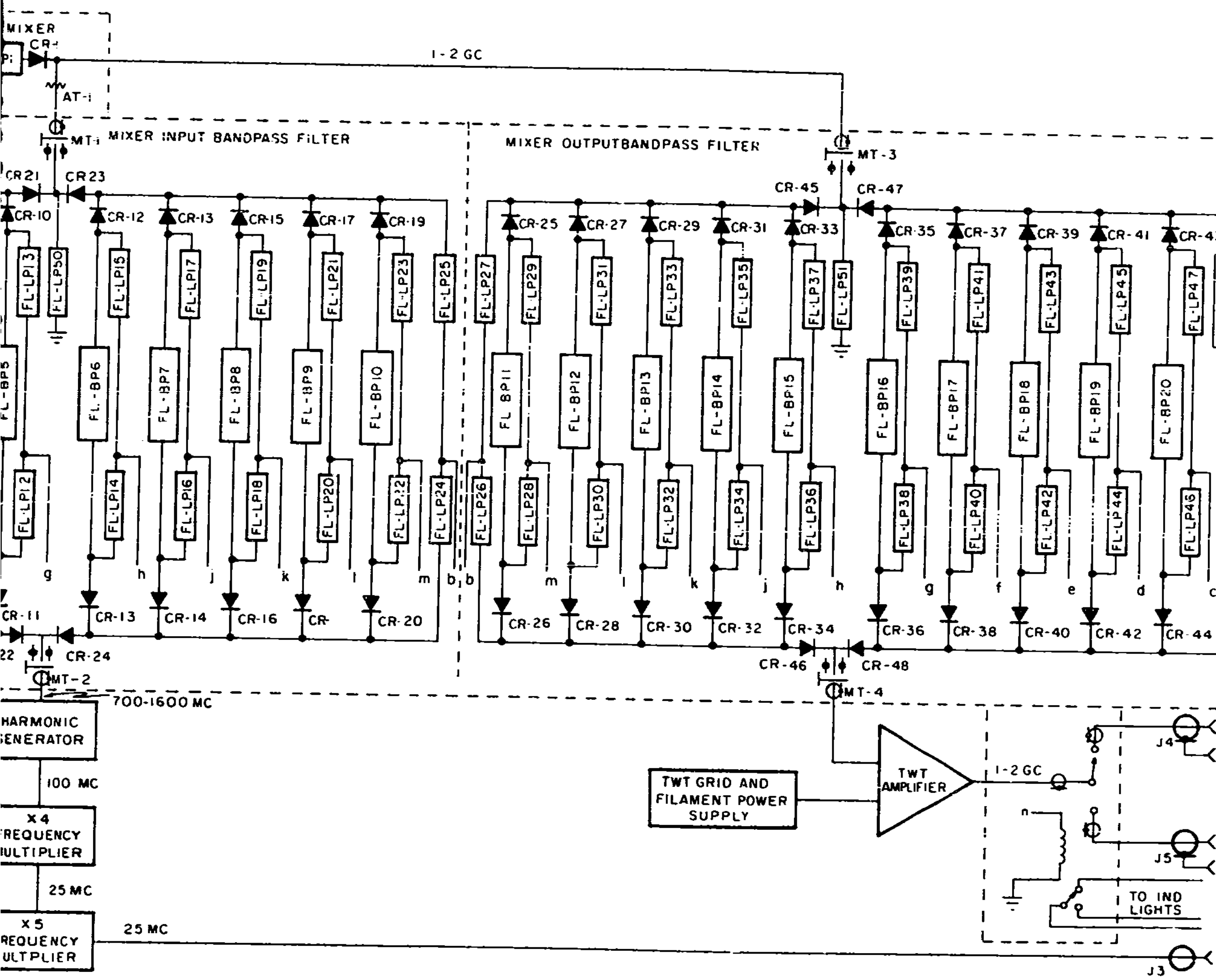


Figure 6-5. L-band frequency extender - block diagram

2

c. Mixer Assembly

(1) Progress and Status

In addition to the external bias specified in the previous quarterly to aid in rejection of spurious signals and enhance the low-level operation of the mixer, DC shorts have been added to the two high-frequency ports of the mixer. The purpose of these DC shorts is to complete the DC path for control of the input and output diode switches.

(2) Plans

The mixer assembly tests will be completed and the unit released for manufacturing during the next quarter.

d. Bandpass Filters

(1) Progress and Status

A final set of dimensions was determined for the wide bandpass filters and a set of printed waveguide wide bandpass filter units is being built. The new designs incorporate quarter-wave stubs from each end of each unit to provide for injection of control bias for the diode switches.

(2) Plans

The units will be tested and released for manufacturing during the next quarter.

e. TWT Amplifier

(1) Progress and Status

Evaluatic of the TWT's of several suppliers was made. The Sperry model STL-222 w s chosen for its availability, price, reliability, low electrode potential requirement and high across-the-band gain. One tube was ordered and received. Engineering evaluation on this tube is now is progress. On the basis of favorable preliminary tests the tube has been released to manufacturing.

(2) Plans

During the next quarter, further evaluation tests will be made to determine the need for grid control to provide leveling of the output power.

f. TWT Bias and Filament Power Supply

(1) Progress and Status

The grid and filament power supply for the TWT has been designed. It consists of a bias source continuously adjustable from -75V to +75V DC and regulated to 1%. The DC filament supply is adjustable 0 to 7.5V and regulated to 2%. The unit also provides an overload protection for the TWT, removing the primary power whenever the helix or cathode currents exceed their specified value. The circuit will recycle every 5 seconds until the primary power is removed. The power supply is presently being fabricated.

(2) Plans

During the next quarter, the power supply will be tested and released for manufacturing.

g. Signal Sampler

(1) Progress and Status

A commercial unit for signal sampling has been specified and ordered. This unit will be used to monitor the output power of the TWT amplifier. During the next quarter tests will be conducted to determine its characteristics with respect to frequency and the associated requirements for its use as a power leveling detector.

(2) Plans

This unit will be released for manufacturing during the next quarter.

h. Output Switch

(1) Progress and Status

The SPDT coaxial switch specified for switching the output power either to the L-band conversion circuits or to the microwave synthesizer is a standard unit used elsewhere in the system. It incorporates a light indicator circuit and a resistive circuit to reduce the high coil closing current to a lower holding value.

(2) Plans

To release the switch for manufacturing.

C. L-Band Conversion Circuits

A block diagram of the L-Band Conversion Circuits is shown in Figure 6-6.

a. Single-Sideband Modulator

(1) Progress and Status

As previously reported, three broad band magic tees are required, and attempts were made to produce these in TEM line. The sketch of Figure 6-7 shows the design used (Ref. E. M. T. Jones "Wide-Band Strip-Line Magic-T", IRE Transactions of MTT, March 1960).

When tested, the best isolation obtained was in excess of 23 db, but the balance (ratio of the output powers) varied more than 1 db. This unbalance was not acceptable, but further development was not pursued because of developments described in the next paragraph.

During the testing described above, one of RCA's suppliers developed a new broad band magic tee using coax line. This magic tee had an isolation in excess of 45 db and a balance of ±0.1 db. This magic tee is being designed into the SSB modulator and TEM-line magic-tee design efforts have been stopped.

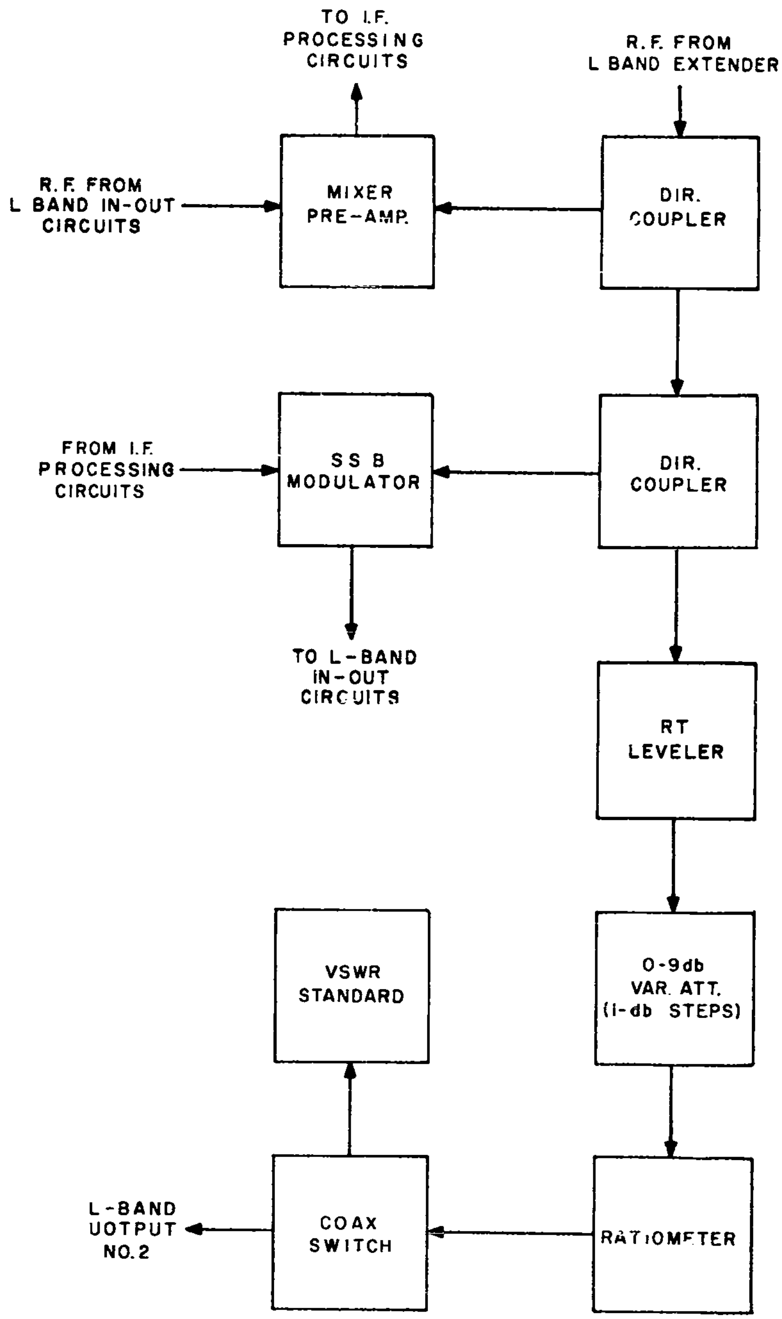


Figure 6-6. L-band conversion circuit block diagram

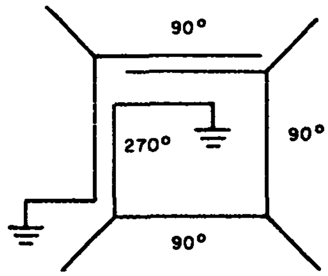


Figure 6-7. Sketch - wide-band strip - line magic T

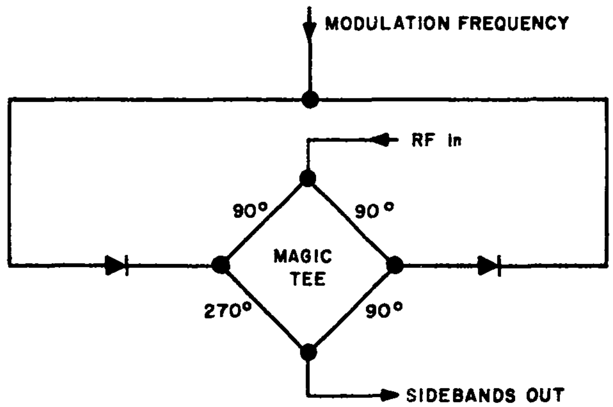


Figure 6-8. Double sideband modulator

A typical conventional double sideband modulator is shown in the sketch of Figure 6-8.

It is necessary to drive the crystals 180° out of phase. This is normally done by placing the crystals in the circuit physically 180° out of phase. Because the RF energy is now incident on physically different ends of the crystals, the phase of one crystal does not track the phase of the other with frequency.

Crystals were then placed in the same direction and modulated 180° out of phase. Considerable improvement was obtained, but the circuits must still be optimized with respect to driving the crystals 180° out of phase.

(2) Plans

Complete circuit optimization; release the unit for manufacturing.

b. Ratiometer

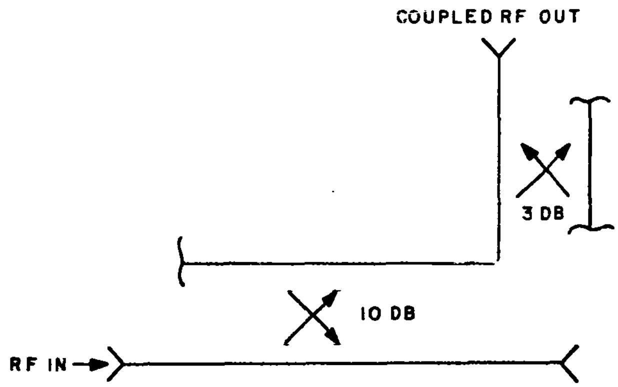
(1) Progres and Status

Because of the method of operation used in the L-Band Ratiometer, a flat high-directivity (≥30 db) coupler was necessary. To date, the only high-directivity couplers available had a 1-db coupling variation. The problem was to flatten this coupler.

This was accomplished by using the insertion loss characteristic of a 3 db coupler to compensate for the coupling variation of the 10 db coupler by adding these two characteristics, resulting in 13 db ±0.3 db coupling with 30 db minimum directivity over the required frequency range. See Figure 6-9.

(2) Plans

During the next quarter breadboard tests will be completed, the error in VSWR readout will be analyzed, and the unit will be released to manufacturing.



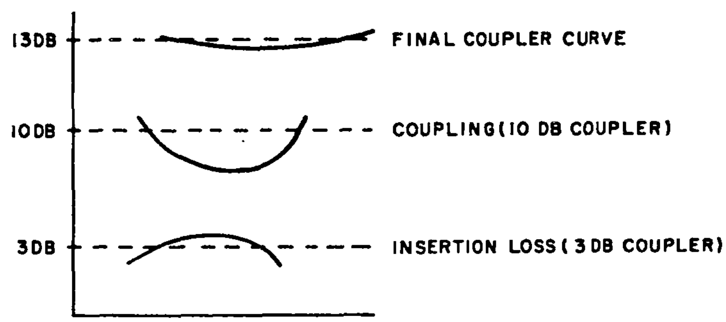


Figure 6-9. Sketch of coupler plus compensating curves to get proper response

c. Variable Attenuator

(1) Progress, Status and Plans

Breadboard activities on this item were completed with satisfactory results. This item will be released to manufacturing during the next quarter.

d. RF Leveler

(1) Status

The power leveler in this chassis is an average-power leveler consisting of a maximally flat coaxial line coupler and a temperature compensating thermistor. The coupler has been received but tests await delivery of the thermistor. It is expected that these tests will be performed during the next quarter, and the unit will be released to manufacturing.

D. <u>L-Band Input/Output Circuits</u>

The simplified block diagram for the L-Band Input/Output Circuits is shown in Figure 6-10.

(1) Progress and Status

The microwave portion of the peak-power leveler has been developed and refined to the point of having only ±0.4 db variation across the band. During the next quarter the microwave and circuitry components will be integrated and tested.

The most severe variable attenuator requirement in the L-band portion of the HF Stimulus occurs as a 0-100 db attenuator in this chassis. A breadboard of this attenuator has been assembled with SPDT switches, transfer switches, precision attenuator pads and preformed rigid coaxial lines. The assembly will be evaluated during the next quarter.

The input power monitor has been changed to incorporate a diode chopper and a bolometer detector. This change has been made to improve the sensitivity of this monitor to facilitate insertion loss measurements of UUT's.

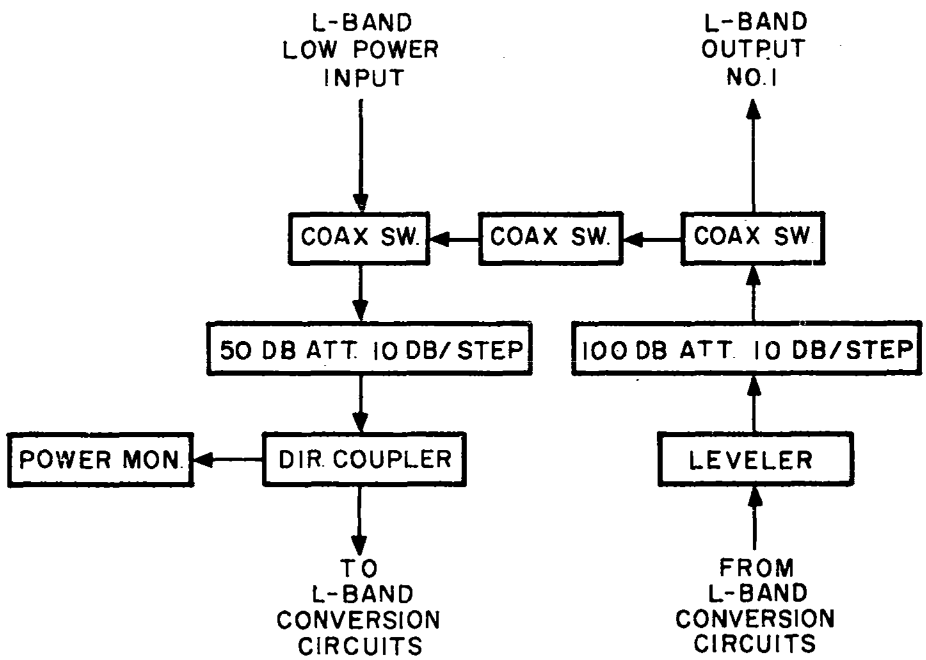


Figure 6-10. L-band input/output circuits - block diagram

(2) Plans

The release of all L-Band Input/Output Circuit designs will be made early in the next quarter.

E. L-Band Dummy Load

(1) Status

Quotations on this unit have been received and are being evaluated. During the coming quarter the selected unit will be released for manufacturing.

F. Microwave Synthesizer

A block diagram of the Microwave Synthesizer is shown in Figure 6-11.

Major effort during this reporting period was directed toward solving the mixer problem discussed in the previous report. To minimize the spurious outputs, the mixer drive level had to be reduced. Since this also reduced the power output at the desired sideband, it was necessary to include a TWT in this chassis to provide sufficient power in the 2-4 Gc band.

a. Mixers

(1) Progress and Status

The mixer configuration has been finalized. Both the 2-3 Gc output and the 3-4 Gc output mixers will have the same configuration. These will be balanced mixers utilizing coax magic tees at the input and the output. The 1-2 Gc swept signal will be fed through the tee to reach the crystals in phase. The fixed frequency (1 Gc on the 2-3 Gc mixer or 2 Gc on the 3-4 Gc mixer) will be fed to the crystals 180° out of phase. Thus the desired sidebands generated at the two crystals will be 180° out of phase and will be coupled out at the out-of-phase port on the output magic tee. The second harmonic of each of the input signals will be in phase in the two arms and will therefore be terminated at the in-phase port of the output magic tee. The 1-2 Gc swept signal will likewise be terminated. Laboratory tests indicated insufficient rejection of the

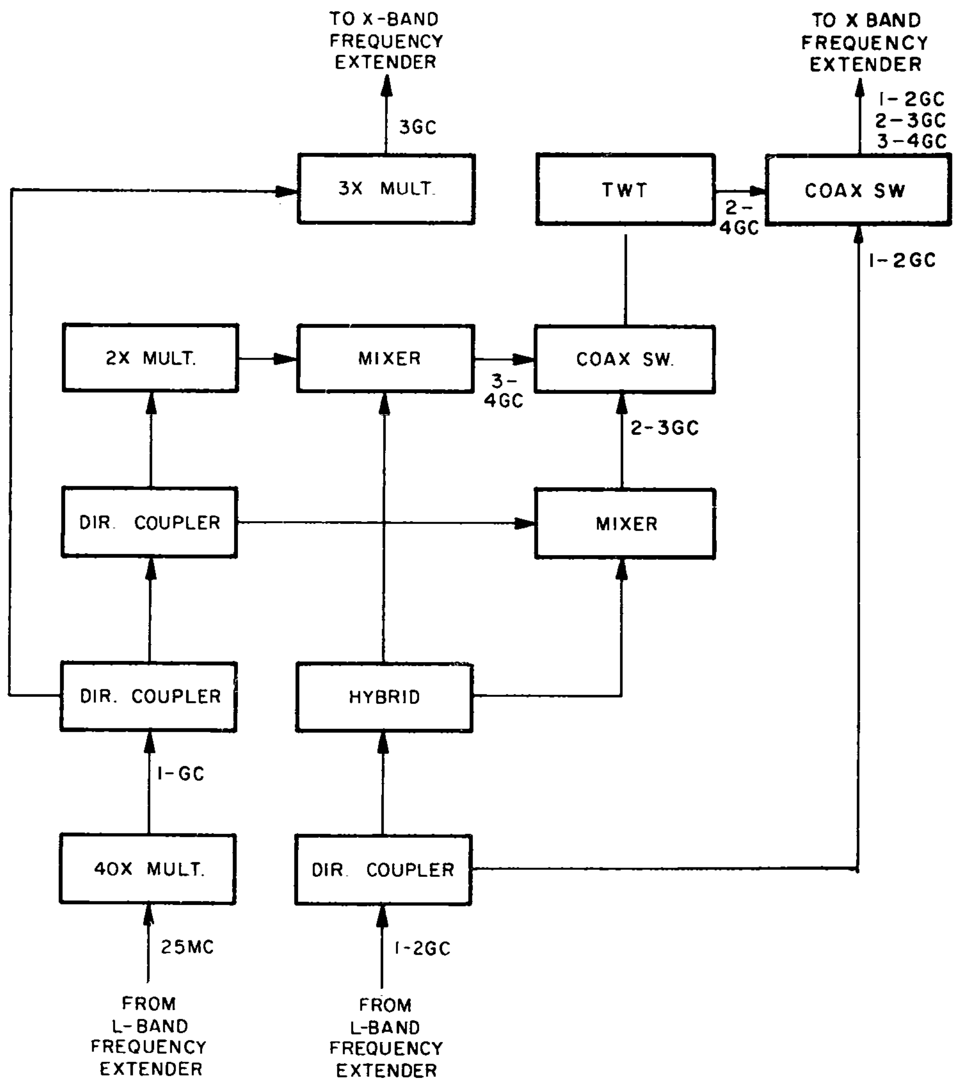


Figure 6-11. Microwave synthesizer - block diagram

1-2 Gc swept frequency at 2 Gc. To eliminate this in the 2-3 Gc output, a 2.5 Gc cutoff high pass filter will be switched into the output line at the midpoint of the sweep. The 2-3 Gc mixer produces a minimum power output of -25 dbm with a maximum variation of 3 db across the band. The maximum spurious response is -44 dbm. The 3-4 Gc mixer produces a minimum power output of -28 dbm with a maximum variation of 3 db across the band. The maximum spurious response is -46 dbm. These results are satisfactory. Greater spurious response rejection is not required, but can be obtained by the use of magic tees which have a better balance across the band. Improvements in magic tees are being investigated; these investigations will continue during the next quarter.

(2) Plans

During the next quarter the mixers will be released for manufacturing.

b. Multipliers

(1) Progress and Plans

Packaging of the X40 multiplier was changed slightly to obtain an improved arrangement of the circuits.

Since all circuitry through 500 Mc utilize lumped constant components, it has been placed on one subassembly. Tests on the breadboard of this subassembly showed a power output of 1.6 watts at 500 Mc. Layout of this subassembly is now in progress.

The output doubler, which consists of distributed parameter components, constitutes a separate subassembly. This subassembly has also been breadboarded and is presently being evaluated.

During the next quarter, breadboard evaluation of the X40 multiplier will be completed, and it will be released to manufacturing.

The X2-multiplier breadboard was received late in the reporting period. During the next quarter this unit will be evaluated and released to manufacturing.

The X3 multiplier is a purchased item and is scheduled for delivery to RCA early in the next quarter. During the next quarter it will be evaluated and released to manufacturing.

G. X-Band Frequency Extender

The block diagram of the X-Band Frequency Extender is shown in Figure 6-12.

a. Mixers

Preliminary mixer tests (without final positioning of either the signal low-pass filter and local oscillator bandpass filter) have produced outputs in the range of -10.5 dbm to -17.5 dbm. Spurious outputs under the same conditions are approximately -29.0 dbm or less. It is desired to produce output signals at a power level of -10 dbm minimum and maintain spurious outputs at least 20 db below the desired output. Design effort during the next period will be aimed at realization of higher mixer efficiency and better spurious signal suppression.

Difficulty has been encountered in obtaining a broadband match on the signal input arm of the mixer. The signal arm consists of a coaxial low-pass filter terminated by a 1N415E ceramic cartridge diode which is placed across the narrow dimension of the waveguide. Space limitations do not allow a broadband transformation from the filter line impedance to the mixer diode impedance; therefore, a modification of the signal input arm is under consideration.

A parallel effort using a 63-ohm coaxial-case diode (1N1132) is also being investigated. An impedance transformation from the filter line to the diode can be achieved in a very small length. The waveguide will be tapered down to an impedance of 63 ohms in the vicinity of the coaxial line. Local oscillator injection is expected to be accomplished through the utilization of a low impedance radial choke preceding the mixer diode.

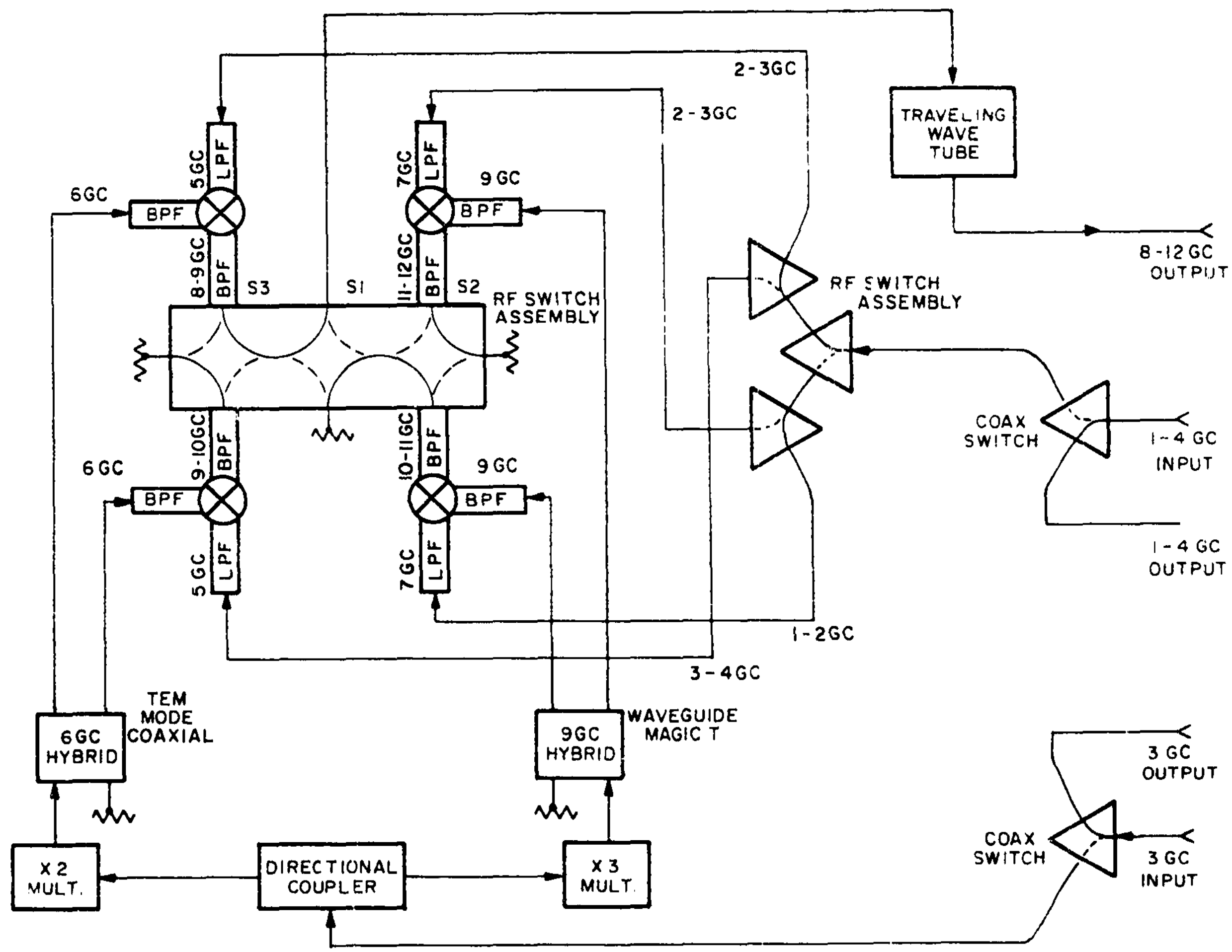


Figure 6-12. X-band frequency extender - block diagram

b. Bandpass Filters

The waveguide bandpass filters were designed with the objectives of obtaining large bandwidths, small ripple (0.1 db), and very little insertion loss within the passband. Preliminary test data showed that the filters lacked bandwidth and adequately small ripple. Since it appeared that the difficulties arose because of improper correction for iris thickness, four jigs were built with different iris sizes, and susceptance versus iris size data was taken. This data was used to redesign the filters and to construct and test one filter. This test data showed excellent bandwidth, very good ripple (less than one db), and insertion loss within the passband of approximately 0.5 db. In the next quarter, the other filters will be built and tested.

c. TWT Filament Supply

The TWT filament supply was breadboarded and the circuit design was completed.

The X2 and X3 multipliers are on order. These had been scheduled for delivery during the current quarter; they are now expected early in the next quarter.

The TWT was received and checked out with laboratory power supplies. Tests with MTE power supplies will be performed during the next quarter.

Design of the X-Band Frequency Extender will be completed during the coming quarter. The only areas requiring further design and breadboarding are the mixer improvements and finalization of the filters. The unit will be released to manufacturing during the coming quarter.

H. X-Band Conversion Circuits

a. Progress and Plans

The block diagram and mechanical layout of the X-Band Conversion Circuits have been modified since the previous quarterly reporting period. See Figure 6-13.

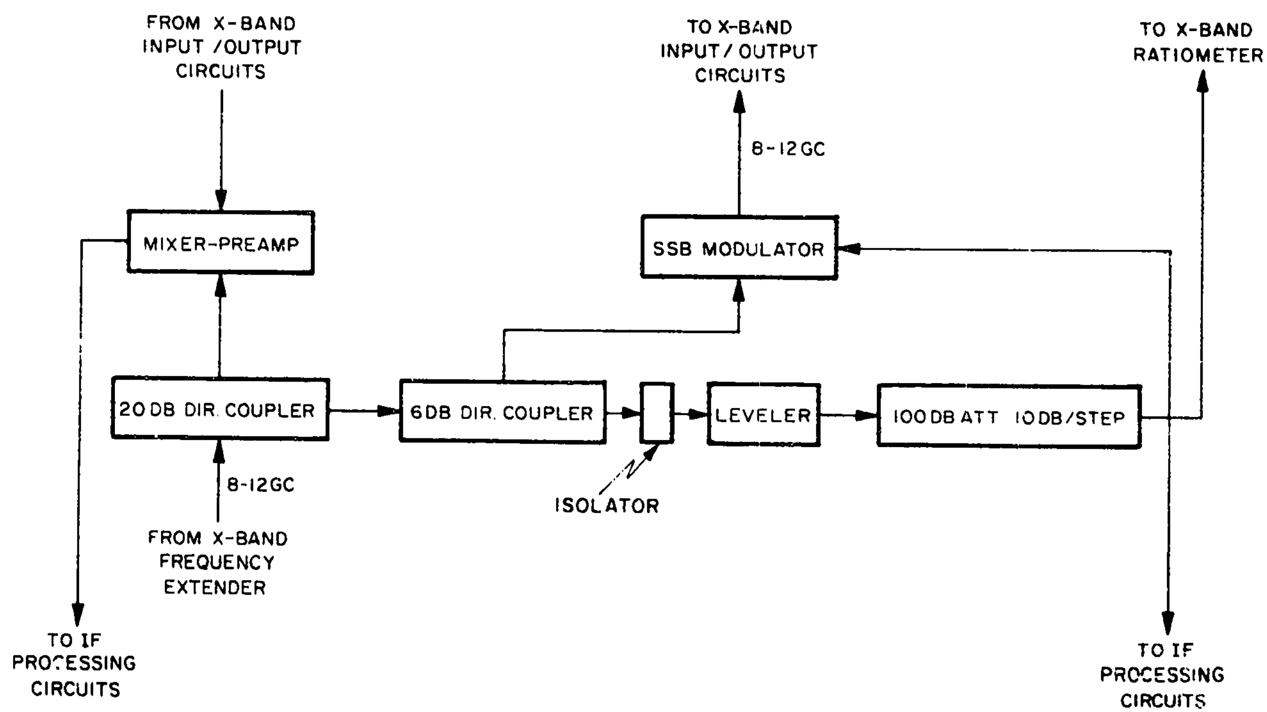


Figure 6-13. X-band conversion circuits - block diagram

(1) The input 10-db directional coupler has been replaced with a 20-db coupler.

(2) The single-ended mixer has been replaced by a balanced mixer which affords suppression of spurious signals from the X-Band Frequency Extender.

(3) The ferrite variable attenuator controlling the input rf power level preceding the SSB Modulator has been moved to the output of the SSB Modulator. This unit will be located in the X-Band Input/Output chassis. Since the SSB Modulator is itself an RF leveler, to accomplish the necessary 10-db variation in translated signal power required an input RF power variation in excess of 20 db. This extended dynamic range did not produce the necessary carrier suppression from the balanced modulators.

(4) An isolator has been inserted between the 6 db coupler through arm and the leveler to protect the TWT in the X-Band Extender from possible high VSWR at the output of the Ratiometer.

(5) The variable ferrite attenuator used in the control loop of the Leveler (see Figure 6-14) has been tested and evaluated. Test results indicate the attenuation versus drive current characteristic varies with operating frequency, but has the positive slope necessary for proper leveler operation. Actual values of attenuation will be controlled by the leveler feedback loop, thus eliminating the frequency sensitive characteristic of the ferrite. The mechanical and electrical operation of the leveler has been modified to permit an increase of power to be available for the Ratiometer. A sample of the cw microwave energy is coupled down by a 10 db directional coupler and detected with a temperature compensated thermistor. This signal is compared to a reference signal and the resultant error controls the attenuation values over a 9-db range in 1-db steps. Work on the breadboard leveler was completed; satisfactory results were obtained.

The special 3-db directional coupler ordered for the microwave quadrature processing portion of the SSB Modulator has been evaluated and operates satisfactorily. Integrating the coupler into the SSB Modulator package and evaluating

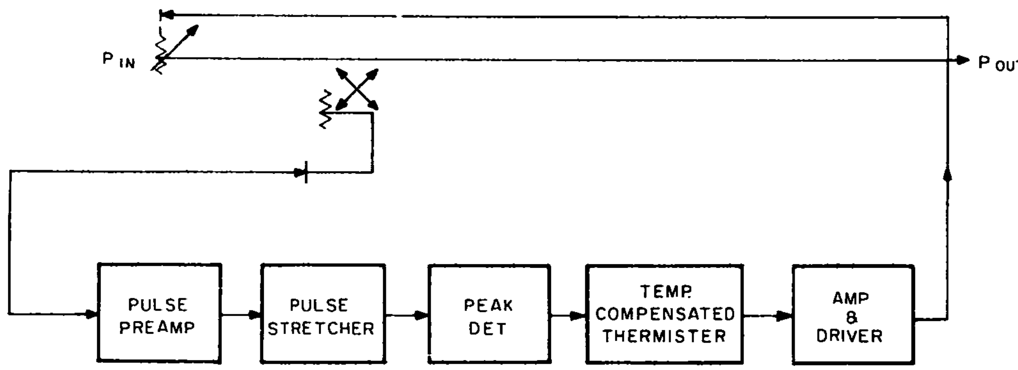


Figure 6-14. X-band RF leveler

this technique for producing a translated single sideband output that tracks the input frequency without additional tuning elements, indicates the feasibility of this approach. Although with ideal components this technique should be applicable across the entire band, satisfactory results were obtained for approximately 20% of the band. Outside this range, performance degraded such that the unwanted lower sideband was not suppressed adequately. The factor controlling this performance, for normal balanced modulator operation, is the coupling variation with frequency of the 3-db coupler which directly affects the output sideband structure. Since the SSB Generator is a reciprocal device, the same result can be obtained by inserting the RF into the 3-db coupler and obtaining the desired sideband spectrum out of the magic tee. Under this condition, the output sidebands are not directly affected by the coupler frequency sensitivity. Operating with rf into the 3-db coupler, the same deviation (1.6 db maximum) in power split is present, but now this variation is applied to the balanced modulators. Each modulator produces a leveling action so the initial input variation is greatly reduced in output sideband deviation. For an input unbalance of 1.6 db to the balanced modulators, the output sidebands change approximately 0.5 db. This smaller deviation produces a tighter control for suppression of the undesired lower sideband. Further tests of the SSB Modulator showed that there were discontinuities in carrier suppression in the 8.5 to 9.8 Gc frequency range. This phenomenon is being investigated for each balanced modulator configuration to determine its origin.

Additional tests of the Sage 1031 tripolar detector mounts with the same properly terminated (1N1132) crystal installed, indicated a change of VSWR with frequency from about 8:1 at 8 Gc to as low as 1.25:1 at 12.5 Gc. The effect of the higher VSWR at the lower microwave frequencies results in an additional 4 to 5 db increase in conversion loss for a constant input power level. Informing Sage of these results has resulted in modification to the existing design of the mounts. Preliminary test results on a new prototype indicate a nearly constant VSWR with frequency. Delivery of 6 modified mounts is expected early in April.

Using the matched UG-471/U magic tee as the major component of the balanced modulators, the tr cking ability of the terminating elements can be established,

as seen in Figure 6-15. The isolation parameter is the relation of the output carrier to the input carrier signal. For the MTE condition where an approximate 10-db conversion loss is obtained for the output sidebands, with all undesired signals suppressed a minimum of 20 db. the terminating elements should lie within the 30-db isolation locus. During the next reporting period the terminating elements will be matched and operated in the completed SSB Modulator configuration.

The mixer preamplifier was breadboarded and tested; satisfactory results were obtained.

Nearly all items for the X-Band Conversion circuits were released to manufacturing.

During the next quarter, release of the X-Band Conversion Circuits to manufacturing will be completed.

I. X-Band Input/Output Circuits

a. Progress and Status

The block diagram for the X-Band Input/Output Circuits is shown in Figure 6-16.

The power monitor has been redesigned to include a ferrite modulator prior to the detector. The detector has also been changed. The temperature compensated thermistor has been replaced by a bolometer. The modulator-bolometer combination affords increased sensitivity and dynamic range. This change increases the dynamic range of the insertion loss measurements that can be made by an rf substitution method. The power monitor breadboard was constructed, and tests were completed.

The power leveler uses a crystal detector. The circuit has been breadboarded and found to be satisfactory.

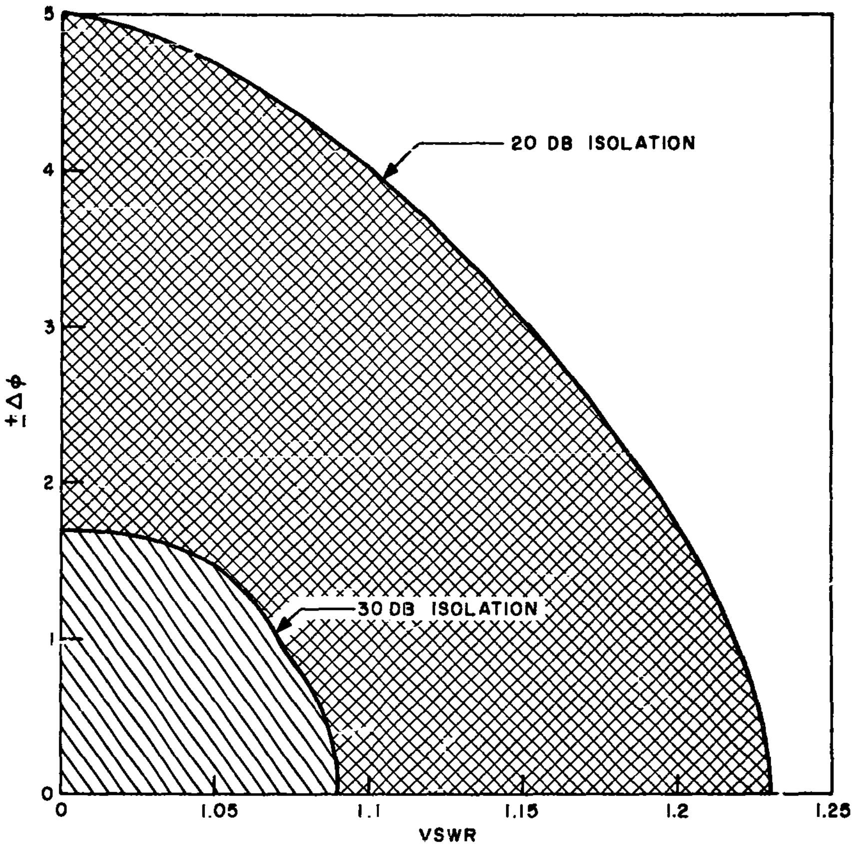


Figure 5-15. Tracking ability of terminating elements

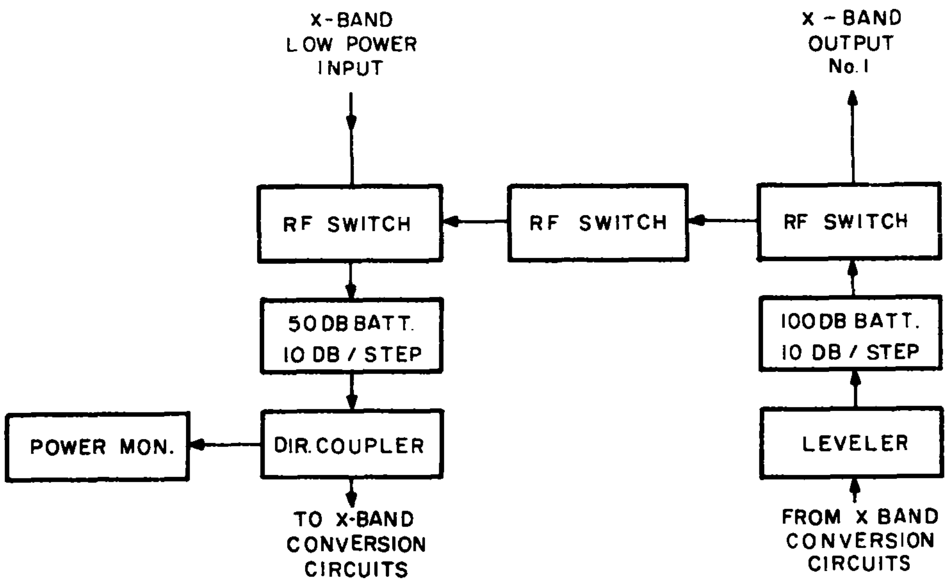


Figure 6-16. X-band input/output circuits - block diagram

Evaluation of the fixed rotary vane attenuator and waveguide transfer switches was completed.

The X-Band Input/Output Circuits assembly was released to manufacturing.

J. X-Band Ratiometer Assembly

a. Progress and Status

The ratiometer performs two functions: (1) It measures VSWR of equipment placed at the output connectors; and (2) measures attenuation (or insertion loss) of a transmission line placed at the output connector. See Figure 6-17.

The basic design approach has remained essentially the same. However, an additional output from the comparator circuit has been provided to the computer to stop attenuator search when the output is closest to zero. This signal is necessary, since nulls which cannot be detected may occur with values of attenuation which are between the 0.5 db attenuator steps.

As previously reported, at the time of a stop search the computer will read out the value of attenuation and convert this to a reflection coefficient. In addition, "go-no go" tests may be made more quickly by programming in a set value of attenuation which corresponds to the highest permissible UUT reflection coefficient. The additional output mentioned above will then provide an indication of actual reflection coefficient of the UUT versus the highest permissible value.

Most of the components have been evaluated, and testing of the breadboard assembly is underway. Satisfactory results have been obtained with respect to the following major characteristics: crystal detector VSWR; voltage output with constant power input; attenuator VSWR and attenuation; and across-the-band evaluation of the standard mismatch.

b. Plans

During the next quarter, component evaluation and breadboard tests will be completed. The main items to be tested are the directional couplers. The X-Band Ratiometer will be released to manufacturing during the quarter.

K. X-Band Dummy Load

Quotations on this unit have been received from outside vendors and are being evaluated. Final decision with respect to cooling (connector versus forced air) has not yet been made. During the coming quarter the design will be finalized and the unit will be released to manufacturing.

L. IF Processing Circuits

The IF Processing circuits in simplified block diagram are shown in Figure 6-18. Two minor changes were made: (1) provisions for two future additional microwave inputs and outputs; and (2) rearrangement of the internal switching.

a. Frequency Search Circuits

The breadboard design has been completed. The stopping accuracy is within 2 Mc of the discriminator zero crossing for a 1-volt rms continuous or pulsed carrier. The mechanical layout of this circuit has begun. The use of the stop search discriminator in the frequency search circuits has been eliminated because it is felt that the adjustment is too critical; a separate discriminator will be used (see c. below). During the next quarter the frequency search circuits will be released for manufacturing.

b. Pulse Modulator

The pulse modulator has been redesigned so that it produces an on-to-off ratio which is greater than 40 db. This was done by using a bridge to balance difference in the capacities of the two diodes used. It is now no longer necessary to use two modulators in series to provide sufficient attenuation in the off mode. Breadboard tests have been completed, and this circuit is ready for mechanical layout. During the next quarter it will be released for manufacturing.

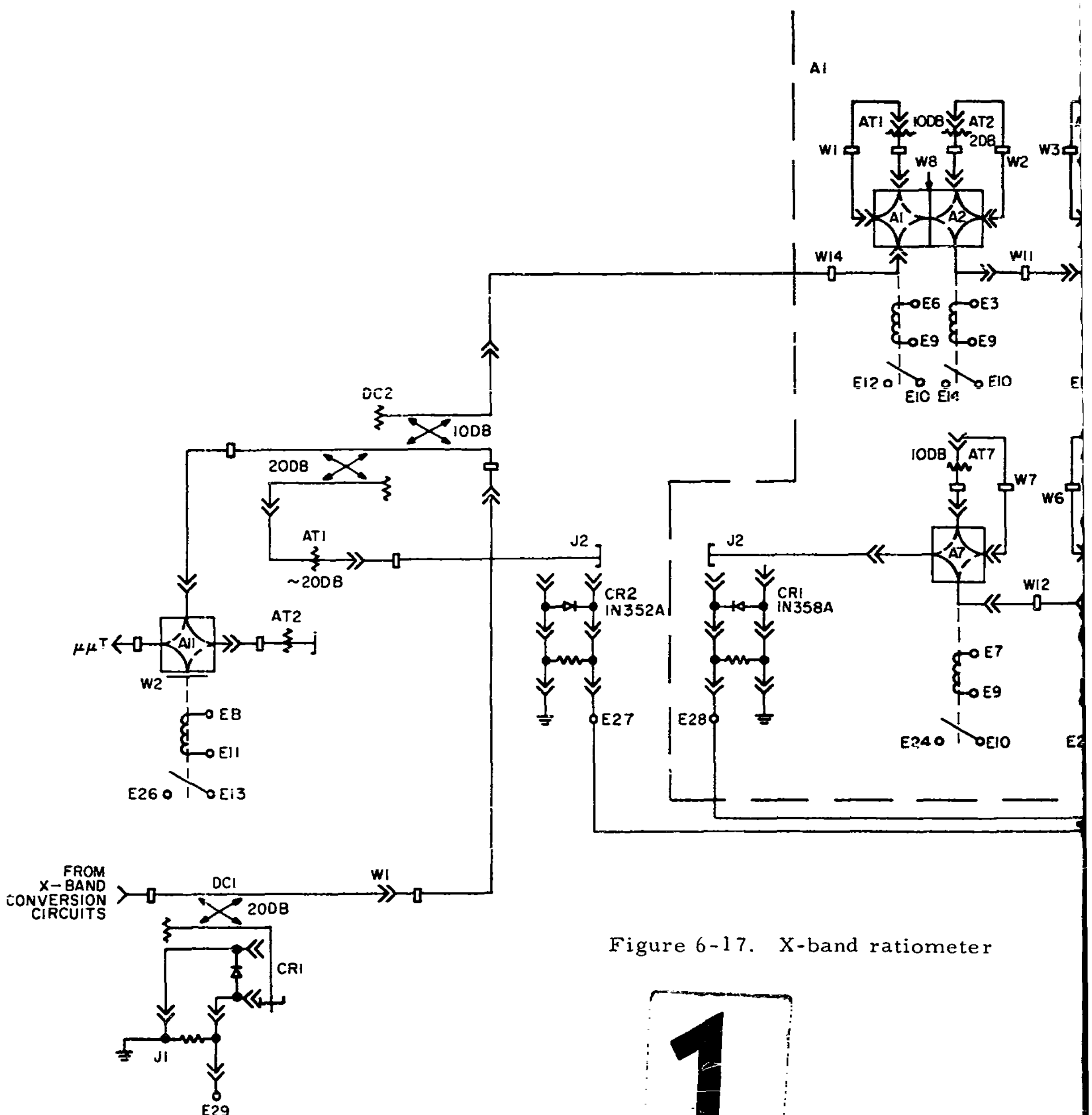


Figure 6-17. X-band ratiometer

1

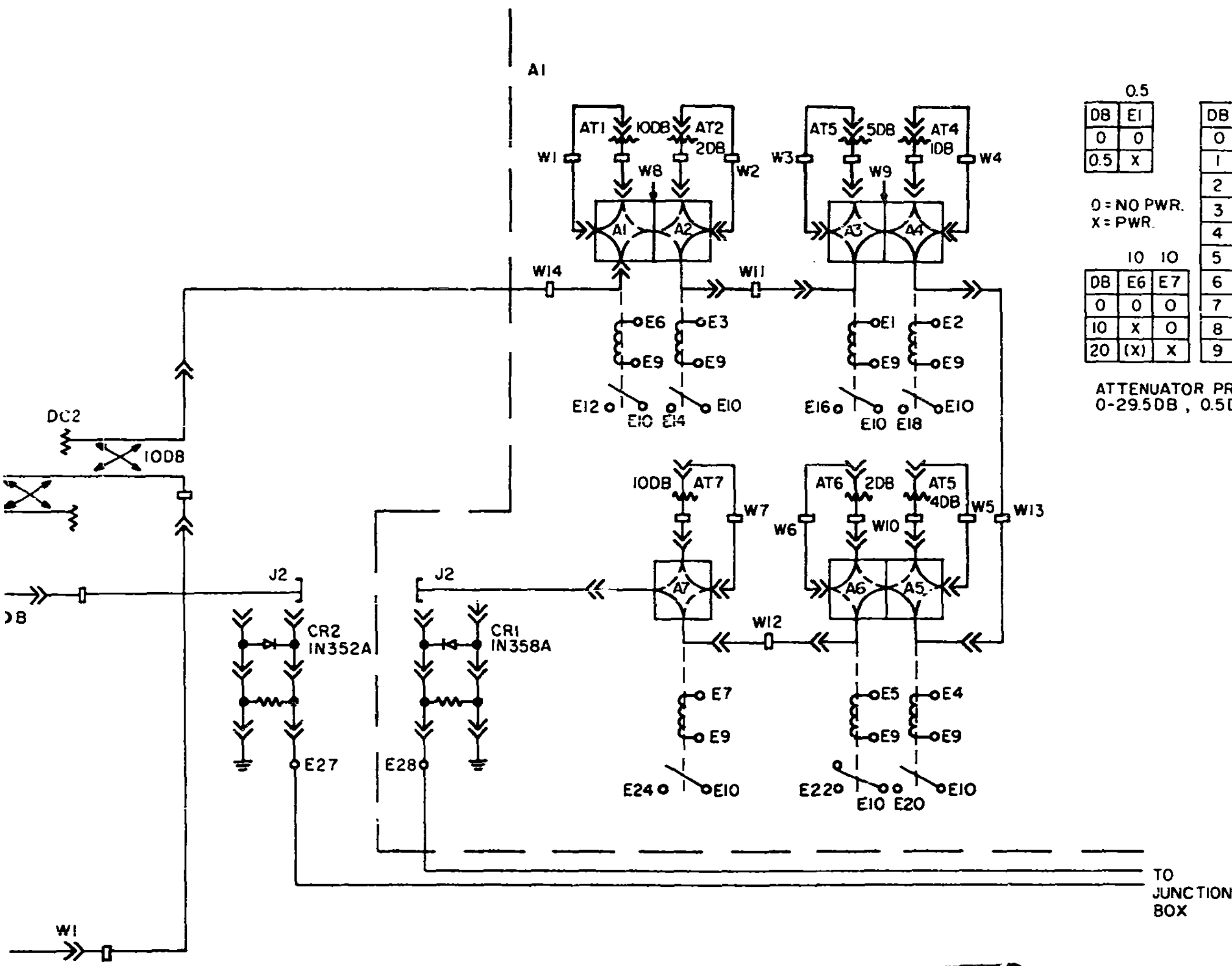


Figure 6-17. X-band ratiometer

	0.5
DB	E1
0	0
0.5	X

0 = NO PWR.
X = PWR.

	10	10
DB	E6	E7
0	0	0
10	X	0
20	(X)	X

	1	2	4	2
DB	E2	E3	E4	E5
0	0	0	0	0
1	X	0	0	0
2	0	X	0	0
3	X	X	0	0
4	0	0	X	0
5	X	0	X	0
6	0	X	X	0
7	X	X	X	0
8	0	(X)	(X)	X
9	X	(X)	(X)	X

ATTENUATOR PROGRAM
0-29.5DB, 0.5DB STEPS

2

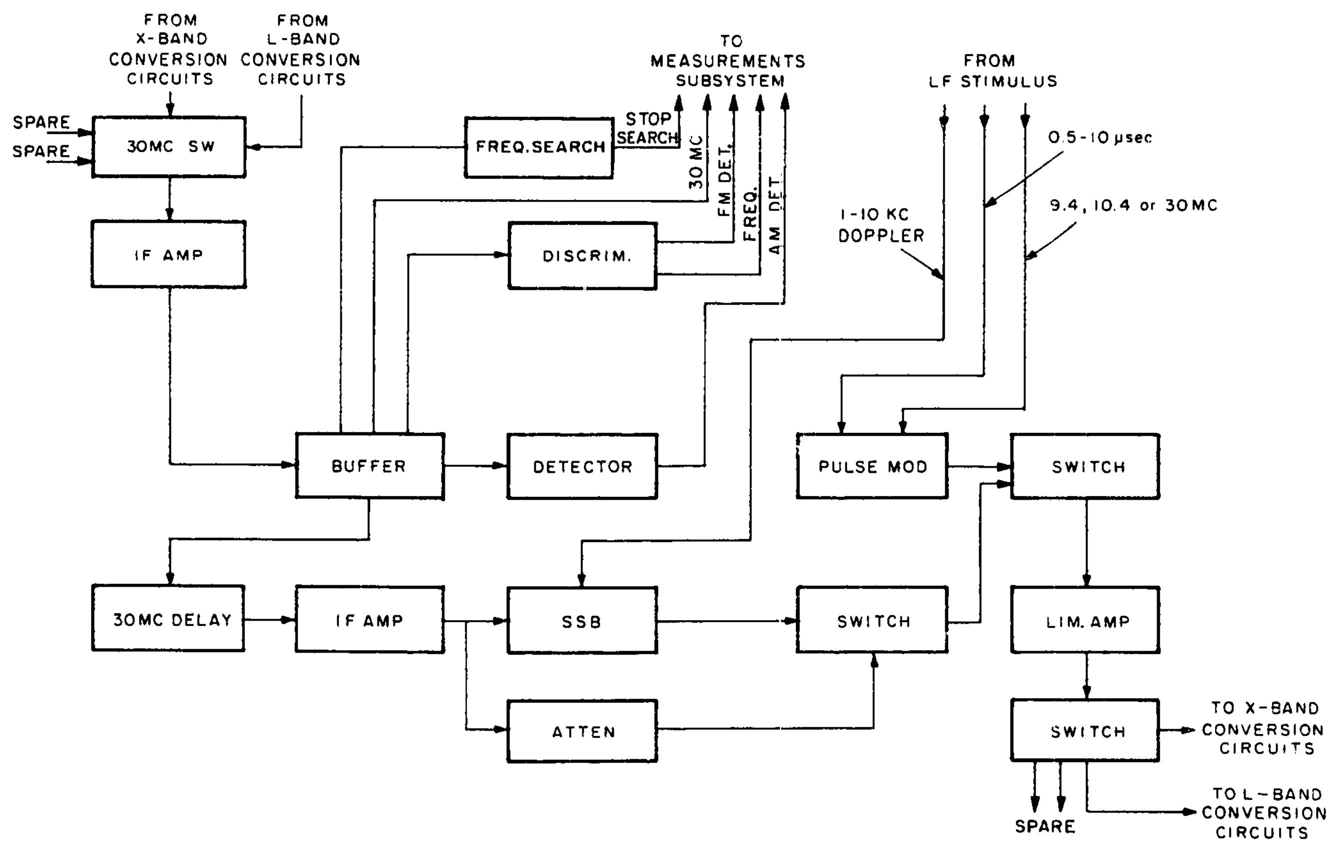


Figure 6-18. IF processing circuits - block diagram

c. Discriminator

Since the stop search discriminator for the FM deviation measurement has been abandoned, a separate discriminator is being designed and evaluated. The new system is self-calibrating and calls for sending a signal with known deviations into the discriminator and generating the UUT deviation signal based on comparison with the known deviation. During the next quarter breadboard test and evaluation will be completed and the discriminator will be released for manufacturing.

d. Limiter Amplifier

The limiter amplifier has been breadboarded and then rebuilt in a preliminary mechanical layout. Test results were satisfactory. It has a bandwidth of 8 to 40 Mc. The output is 1 volt rms for all inputs exceeding 10 millivolts rms. During the next quarter the limiter amplifier will be released to manufacturing.

e. 30-Mc Single Sideband Generator

The single sideband generator has been completely breadboarded. All spurious signals (for a carrier input of 20-40 Mc and Doppler shift input of 1-10 kc) are 25 db down. Some difficulty with short pulse operation was experienced in the original balanced modulators used. These balanced modulators used the same polarity diodes with parallel input for the carrier and push-pull input for the Doppler shift. It was difficult to provide balanced Doppler push-pull input and also provide a balanced load for the detected video pulses from pulsed cw input. It was therefore necessary to use reversed diodes. The rf was then provided as push-pull and the Doppler input as single ended. The detected video load was then essentially the same for each polarity and the operation for pulsed cw input was satisfactory. Mechanical layout of the single-sideband generator has been started; during the next quarter it will be released for manufacturing.

f. 30-Mc Delay Line

The 30-Mc delay line was ordered and received. The vendor took no exceptions to the specifications. Preliminary electrical measurements indicate that the

delay line performs to specifications; during the next quarter measurements will be completed and the line will be released to manufacturing.

g. 30-Mc IF Amplifier

The 30-Mc IF amplifier has been breadboarded. It has 50 db gain with a bandwidth of 20-90 Mc. The maximum output level is slightly over 1 volt rms into 50 ohms, which is sufficient to drive the single-sideband modulator. Mechanical layouts have begun on the 30-Mc IF Amplifier; during the next quarter this amplifier will be released for manufacturing.

The 30-Mc IF amplifier which follows the 30-Mc switch differs from the other 30-Mc IF amplifier in that it includes AGC. During the next quarter this amplifier will be breadboarded, evaluated, and released for manufacturing.

M. Traveling Wave Tube Power Supply

a. Progress and Status

The electrical design of the high-voltage traveling wave tube (TWT) supply was completed and construction of the breadboard unit was begun. The description given in the previous quarterly progress report generally still applies, but a few minor changes have been made.

Overvoltage protection is still provided, but the output high voltage, not the input, will be monitored; the helix current and the cathode current will also be monitored. Any fault (either excessive current or excessive voltage) will shut off the high voltage for five seconds. The supply will continue to recycle until the primary power is removed.

The corona type voltage regulators have been eliminated because of wide voltage variation with temperature which results in a 3% deviation in the output voltage. A new design in which the output voltage is divided down by a factor of approximately one hundred and applied to a low drift differential amplifier has been incorporated. The drift of the amplifier is not expected to exceed one millivolt which will result in a one-tenth volt variation at the output (0. 01%).

b. Plans

During the next quarter breadboard construction and test will be completed, and the unit will be released to manufacturing.

N. Junction Box

a. Progress and Status

Electrical design was completed during this reporting period. This unit performs frequency decoding for the microwave synthesizer and other frequency dependent switches. Signals to be distributed to more than one chassis in the HF Stimulus subsystem will be amplified and distributed through the junction box. No breadboard is required for this unit.

b. Plans

During the next quarter, this unit will be released to manufacturing.

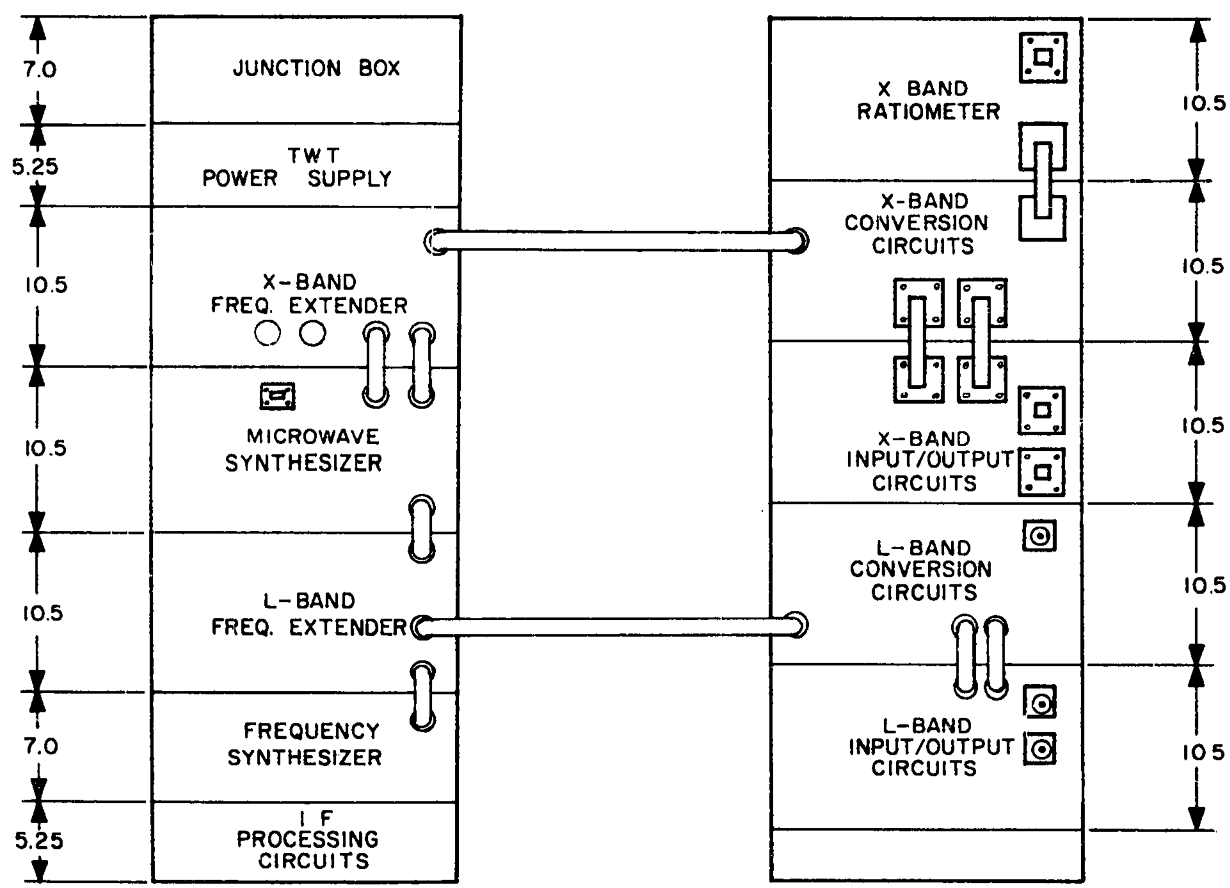
O. Mechanical Design

a. Status and Progress

The overall rack configuration was finalized; the configuration is the same as was shown in the previous quarterly report. See Figure 6-19.

The interconnection diagram showing cabling required in the racks is being prepared and will be completed during the next quarter. High frequency interconnections will consist of waveguide or coaxial components; these were designed during the reporting period.

Layouts for the racks and chassis were started. Approximately 75% of the layouts were completed. Detail drafting was started; approximately 50% of the units were completed.



NOTE: X-BAND LOAD AND L-BAND LOAD ARE EXTERNALLY MOUNTED

Figure 6-19. High frequency stimulus - rack layout

b. Plans

During the next quarter, all detailing will be completed and released tc manufacturing for fabrication.

6.1.4 LOW FREQUENCY STIMULUS

A. Introduction

Several major changes were made in the Low Frequency Stimulus configuration as follows:

(1) The switching which was formerly performed in the individual stimulus generators is now being performed in a new assembly, Stimulus Routing MTE 5894. This decreases the complexity of the controller and programming, and, also decreases the amount of the control hardware required.

(2) The DC/AF Switch has been combined with the Resistance Load, bringing this function closer to the adapter panel.

(3) A synchronizer MTE 5896, taken from the Mauler system, has been added to the complement of Low Frequency Stimulus generators. This will supply Mauler-peculiar requirements for pulses.

(4) Based upon additional information from the Test Requirements Analysis, the Servo Modulator has been removed from the equipment complement.

Figure 6-20 shows the simplified block diagram of the Low Frequency Stimulus. All blocks shown are associated with the Electronic Test Set, except for the 115/10 volt AC power supply which is associated with the Hydraulic Test Group. Two units are yet to be defined; these are the Digital Message Receiver and the Digital Message Generator.

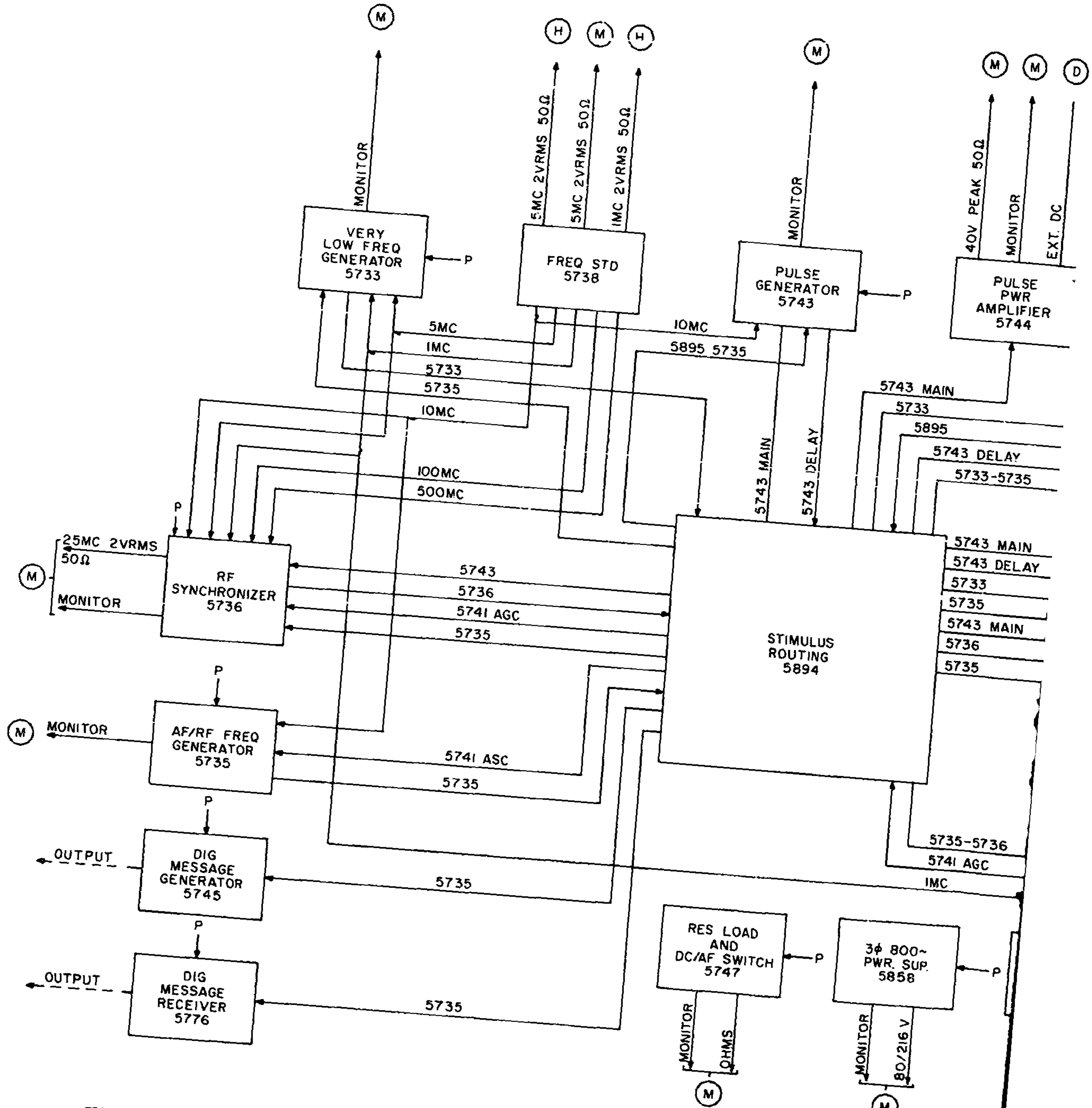
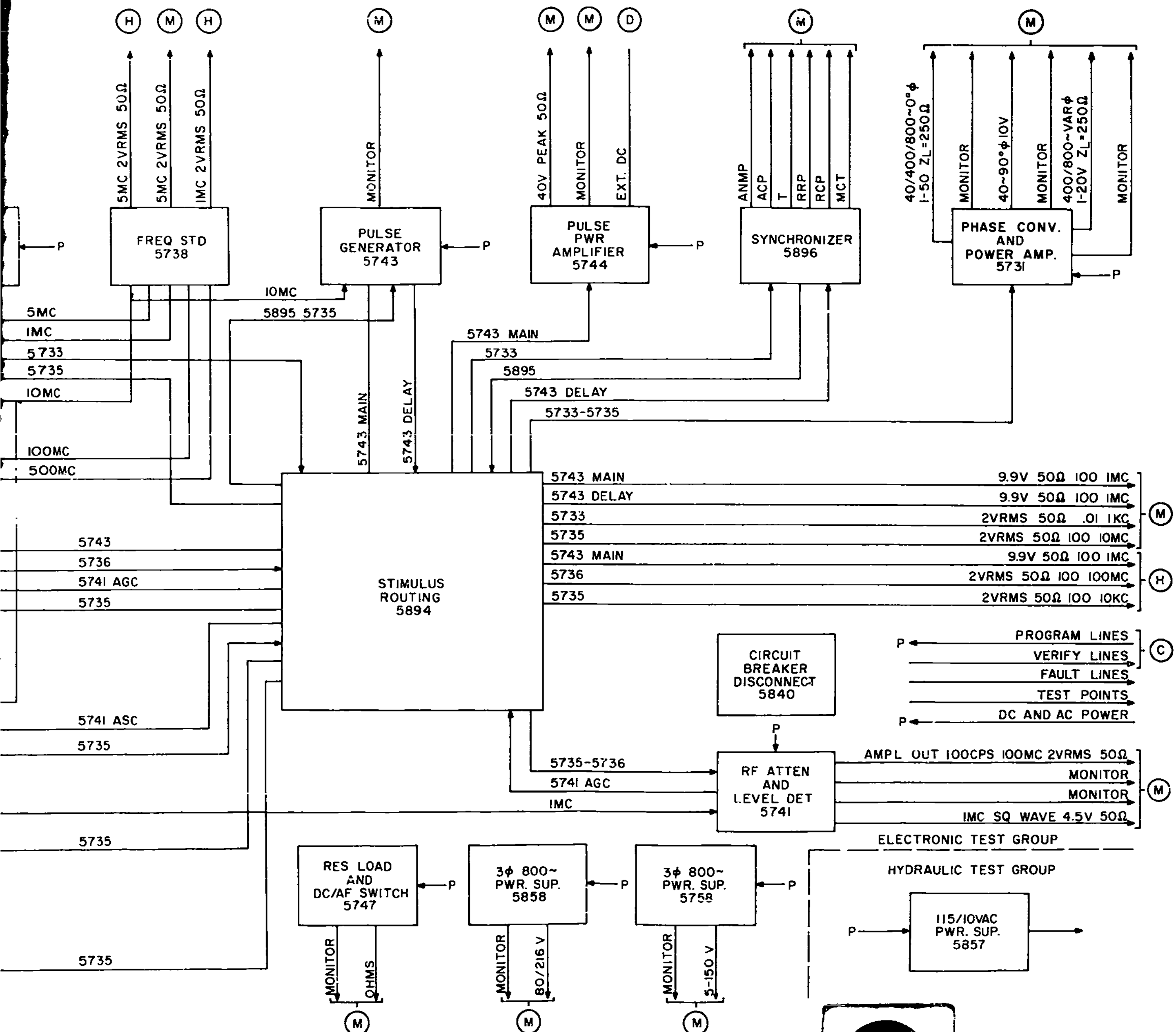


Figure 6-20. Low frequency stimulus - simplified block diagram.

1



uency stimulus - simplified block diagram.

2

6-49/6-50

B. Very Low Frequency Generator

a. Progress and Status

The block diagram, which was not changed during the quarter, is reproduced in Figure 6-21.

The VLF detailed digital logic has been completed. The logic was subdivided into types and quantities of specific circuit boards, and these have been released to drafting for layout. The DACON has been breadboarded and has been found to operate satisfactorily at room temperature. The synthesizing resistors for a sine wave and the solid state switches have been breadboarded and operate satisfactorily at room temperature. Tests on the combination of the solid state switches and the synthesizing resistors are being performed. All mechanical parts and connectors for the chassis were released to manufacturing.

Design and test of the frequency generator circuit to produce the nine internal frequencies from 1 to 9 Mc (which are used in developing the desired output very low frequenc :s) was deferred until the next quarter. When accomplished, this will complet overall circuit design.

b. Plans

(1) The analog circuits, which have been breadboarded individually, will be integrated and tested over the temperature environment.

(2) The VLF design will be completed and will be released for manufacturing.

C. AF/RF Generator

a. Progress and Status

The AF/RF block diagram which was not changed during the quarter is reproduced in Figure 6-22.

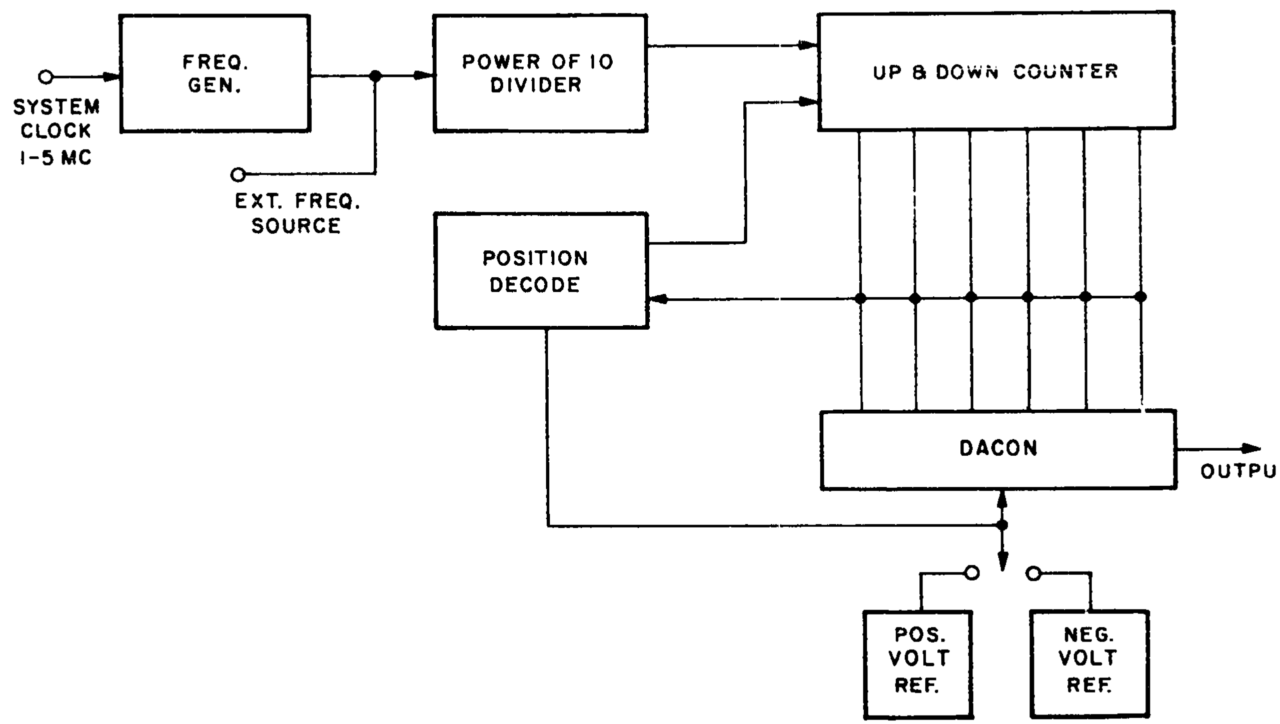


Figure 6-21. VLF generator - block diagram

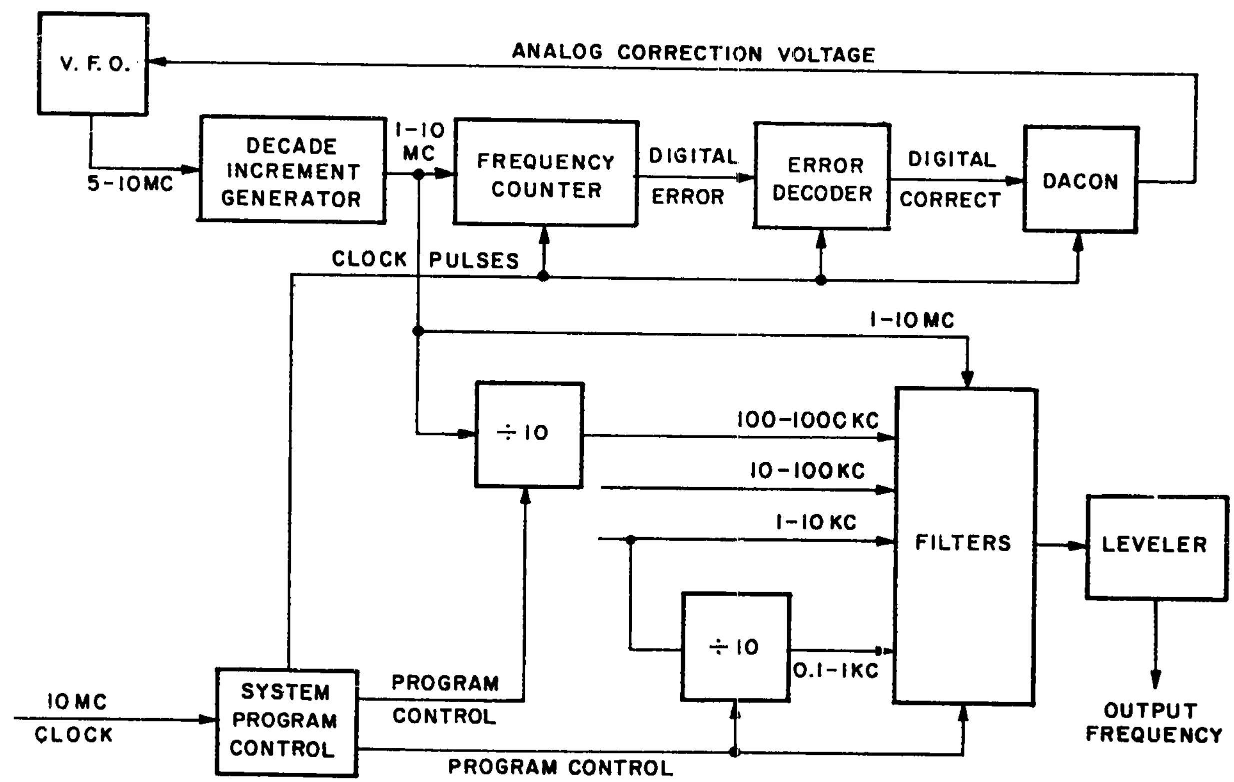


Figure 6-22. AF/RF generator - block diagram

The detailed logic diagram for this unit has been completed. The logic diagram has been subdivided into areas of circuitry which can be conveniently placed on standard printed circuit boards. These have been released to drafting for layout. The m chanical hardware for the unit has been released to manufacturing for fabrication. Breadboard effort startea on the VFO and the associated DACON; the VFO design being breadboarded is the one that carries a 2 to 1 frequency range.

b. Plans

(1) VFO and DACON breadboards will be completed and evaluated.
(2) The output Buffers and Filters will be designed.
(3) Release for manufacturing will begin.

D. RF Synthesizer

a. Progress and Status

Figure 6-23 shows the RF Synthesizer in block diagram form. The Status of the subassemblies in the RF Synthesizer is described below.

1. Harmonic Generators

The design of the 100-kc harmonic generator circuits was completed during the previous quarter. Release to manufacturing is scheduled for the coming quarter.

In the 1-Mc harmonic generator, filter response was improved. Tests over the temperature range from -18°C to +74°C and over the frequency range from 36 to 45 Mc showed satisfactory harmonic amplitudes. This completed design of the 1-Mc harmonic generator; release for manufacturing will be made during the coming quarter.

The 10-Mc bandpass filter is a purchased item. One unit was received during March; it will be tested with the 10-Mc harmonic generator during the

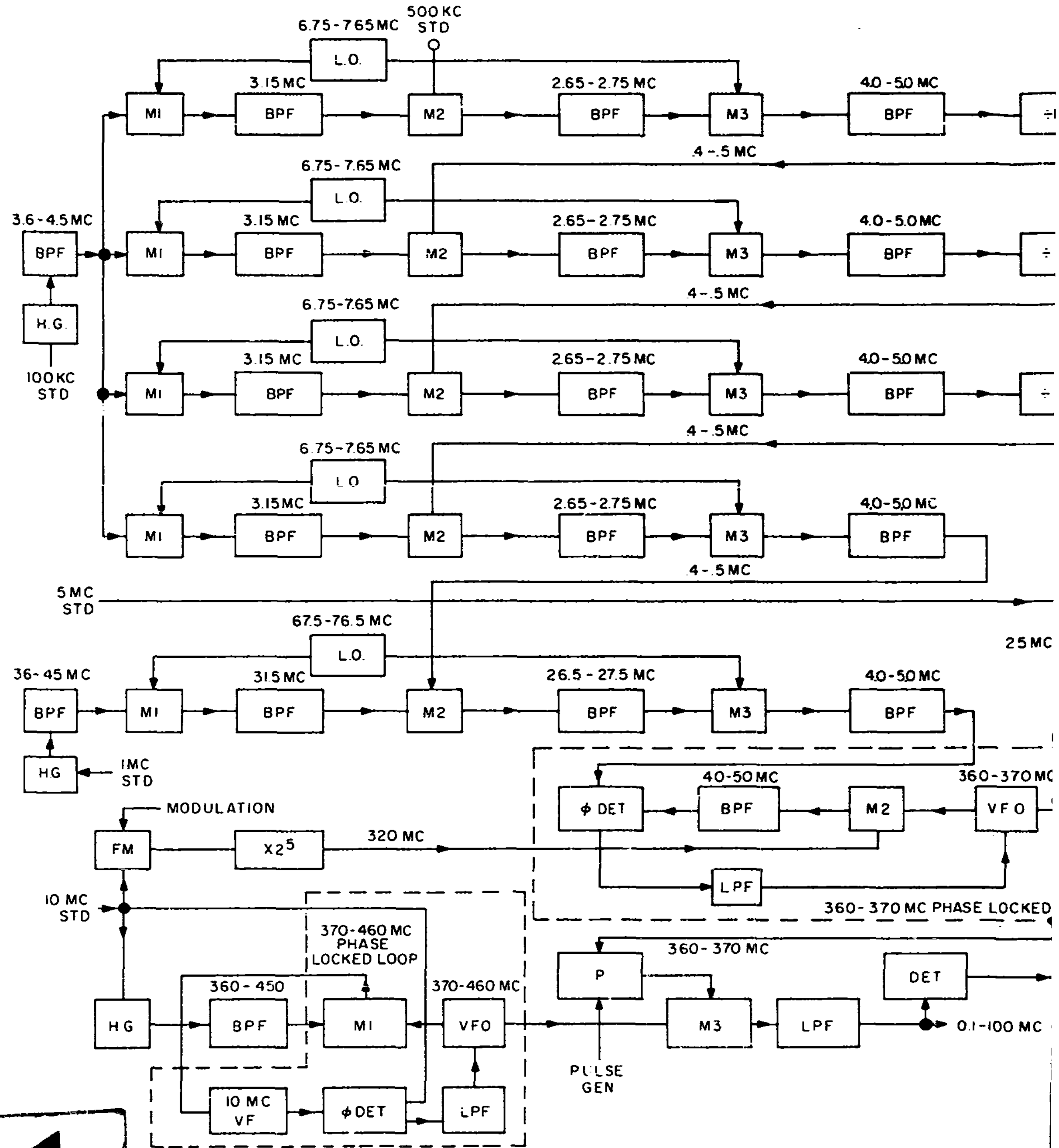
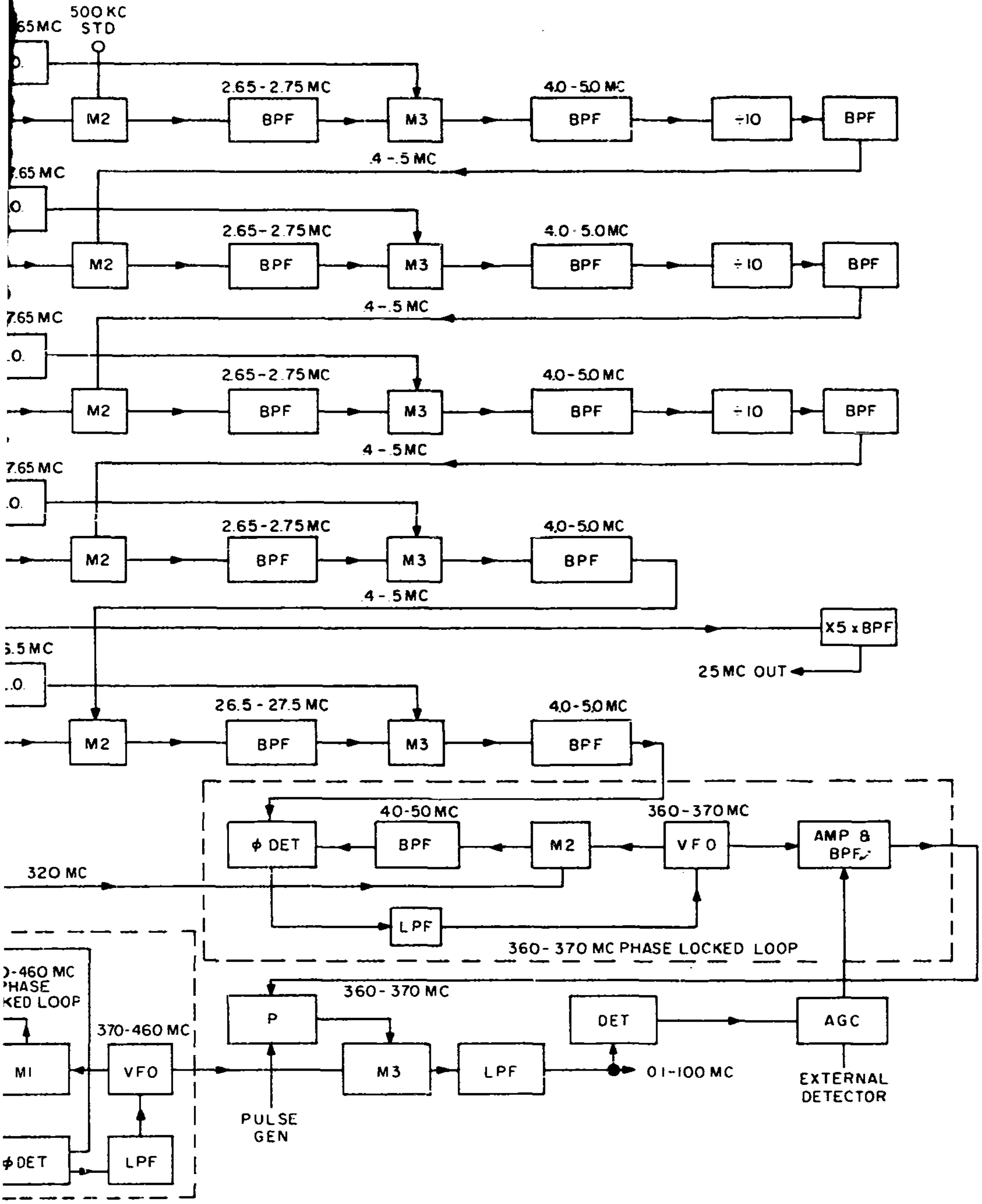


Figure 6-23. 100 Kc to 100 Mc frequency synthesizer



BPF - BAND - PASS FILTER
HG - HARMONIC GENERATOR
LO - LOCAL OSCILLATOR
LPF - LOW-PASS FILTER
M - MIXER
STD - FREQUENCY FROM CENTRAL FREQUENCY STANDARD
VFO - VARIABLE FREQUENCY OSCILLATOR
ϕDET - PHASE DETECTOR
÷10 - FREQUENCY DIVIDER
Ⓘ - ALL BOXES MARKED LPF AND BPF MAY BE EITHER ACTIVE OR NON-ACTIVE CIRCUITS.
FM - MODULATOR FM
P - PULSE MOD.
DET - DETECTOR

2

Figure 6-23. 100 Kc to 100 Mc frequency synthesizer - block diagram

next quarter. The 10-Mc harmonic generator will be released for manufacturing during the next quarter.

2. Mixers

The balanced mixers used in the 100-kc decade circuits were breadboarded. Using a local oscillator signal, f_o, and two-tone modulating signal, f_m, results of initial testing with resistance terminations were as follows: f_m in output, 40 db below lower sideband; f_o in output, 27 db below lower sideband; conversion loss (f_m to lower sideband), 5 db; and intermodulation in lower sideband, -34 db. These results are satisfactory. The 100-kc decade mixers will be released to manufacturing during the next quarter.

The configuration for these mixers is shown in Figure 6-24. Transformers T1 and T2 are two halves of pot cores which are put together after the coil has been wound on a bobbin. The air gap causes unbalance above 10 Mc between the center tap and the two halves of the transformer.

Development of mixers for the 1-Mc decade began. Transistor mixers will be investigated and, probably, diode mixers. Tests on a breadboard mixer consisting of a single transistor and tunable circuits showed that adjustments were very critical because the desired lower sideband and f_m frequencies are very close together. A balanced mixer employing complementary transistors and simple tuned circuits will be investigated during the next quarter. Results of these investigations will permit a decision to be made as to whether transistor or diode mixers will be used. In the event that transformers are required in the balanced mixer for this decade, a wideband transformer has been breadboarded and tested. Results at room temperature were satisfactory. The transformer utilized a toroidal core to overcome the unbalance noted in the transformers for the 100-kc decade. Design of this mixer will be completed during the next quarter and it will be released to manufacturing.

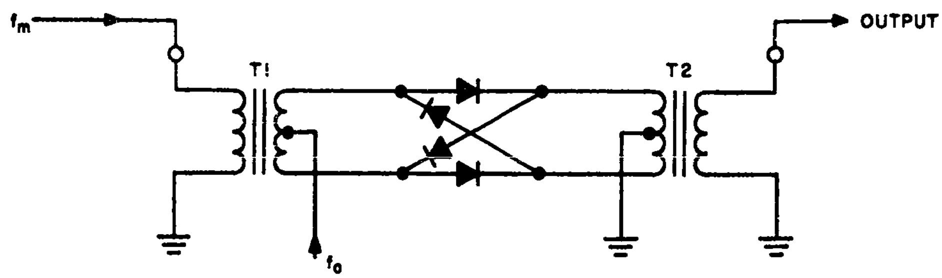


Figure 6-24. Mixer configuration

Development of the mixer for the 10-Mc decade was completed. This is a purchased item. It was ordered, received, tested, and released for manufacturing.

3. Local Oscillators

The Colpitts oscillator described in the previous quarterly report was breadboarded and checked over the temperature range from -20°C to +55°C. Drift in frequency due to variation of varicap capacitance was found to be excessive - the drift exceeded the 20-kc bandwidth of the 3.15-Mc bandpass filter.

The voltage controlled oscillators were therefore replaced by crystal controlled oscillators. Ten crystal controlled oscillators are used to provide 100-kc steps over the range from 6.75 to 7.65 Mc. Drift cancellation circuits are used, hence fine frequency adjustment is not required for temperature compensation. DACONs to supply varicap voltage are no longer required.

Breadboards of the 6.75 to 7.65 Mc local oscillator and the amplifier which follows it were constructed. Breadboard testing began. During the next quarter, tests will be completed, the design will be finalized, and release will be made to manufacturing.

The 67.5 to 76.5 Mc local oscillator is being redesigned to use crystals instead of varicaps. A breadboard was constructed. During the next quarter, breadboard tests will be completed, the design will be finalized, and release will be made for manufacturing. Also during the next quarter, the associated buffer amplifier will be designed, breadboarded, tested, and released for manufacturing.

4. Filters

The improved frequency stability obtained with the crystal oscillators eases the requirements on the 3.15- and 31.5-Mc bandpass crystal filters. These filters are being designed. They will be breadboarded, tested and released for manufacturing during the next quarter.

All other filters in the RF Synthesizer will be LC type. Four of these were designed during the quarter. Design of the remainder is in process, with all scheduled for release to manufacturing during the third quarter of 1963.

5. 10:1 Dividers

A four stage binary counter with standard MTE flip flops is used, followed by a bandpass filter to recover the sine wave. A breadboard was constructed, and tests are scheduled to begin and to be completed during the next quarter. Release for manufacturing is scheduled for the next quarter.

6. 360 to 370 Mc Phase Locked Loop

The breadboard of this loop was completed. Closed loop measurements made at room temperature from 360 to 370 Mc, but without insertion of frequency modulation, showed satisfactory results.

Point of insertion of FM was determined; selection was made between the two methods presented in the previous quarterly report. In one method, the FM signal is converted to a DC signal which is inserted between the phase detector and the low-pass filter. Tests with this approach showed that the loop would not lock in. Hence, the alternative method referred to in the previous quarterly report will be used; in this method, which is shown in the block diagram of Figure 6-23, the FM signal is introduced into the mixer. Construction of the breadboard for this approach began. During the next quarter, the breadboard will be completed and testing will begin. Tests will be completed, and the loop will be released for manufacturing during the third quarter of 1963.

7. 320 Mc Generator

The higher Q varactors for operation at 320 Mc were obtained and placed in the breadboard. Selectivity, harmonic suppression, and efficiency were improved to a satisfactory degree. The 320-Mc generator was released for manufacturing.

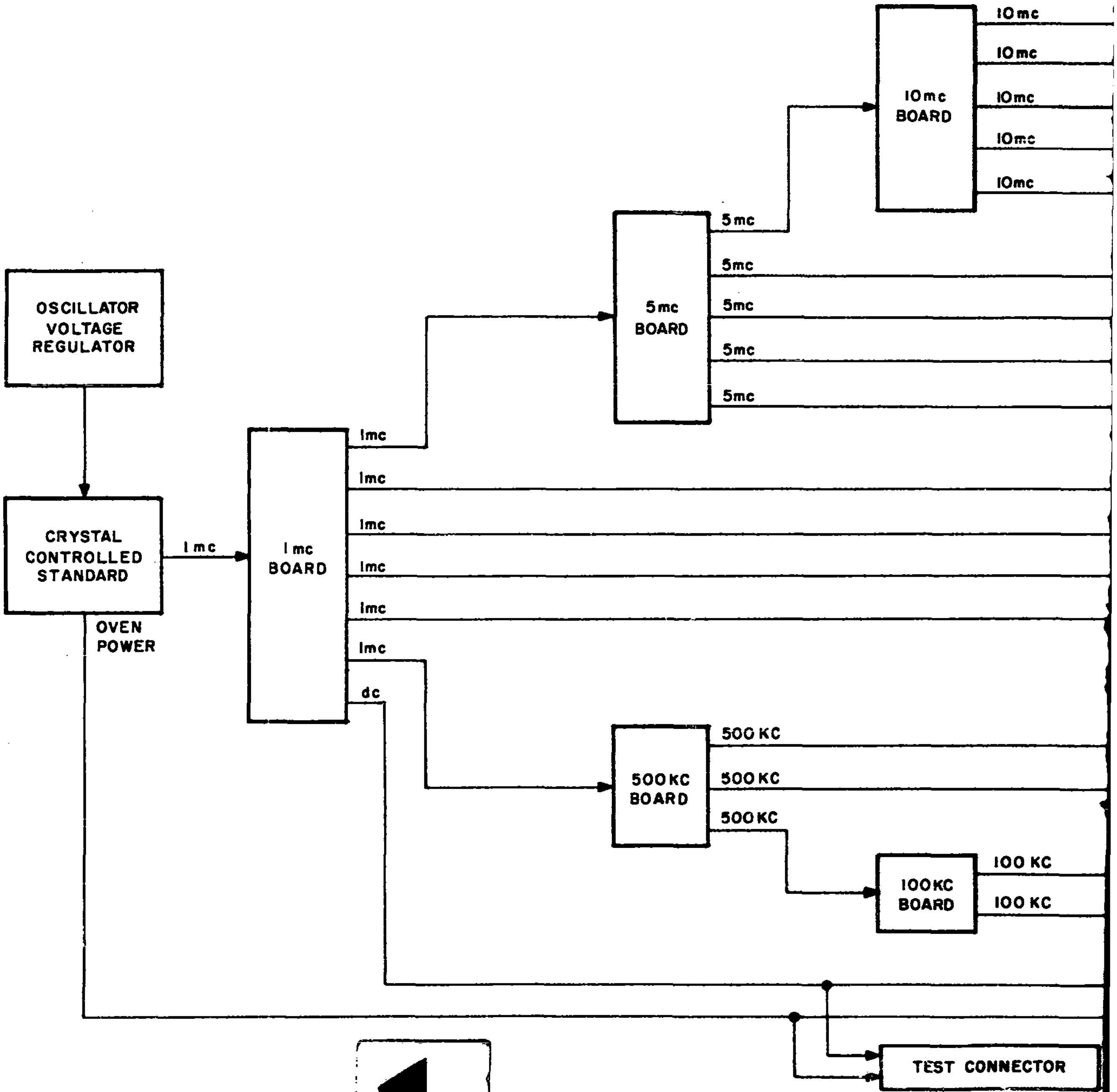


Figure 6-25. Frequency standard - block diagram

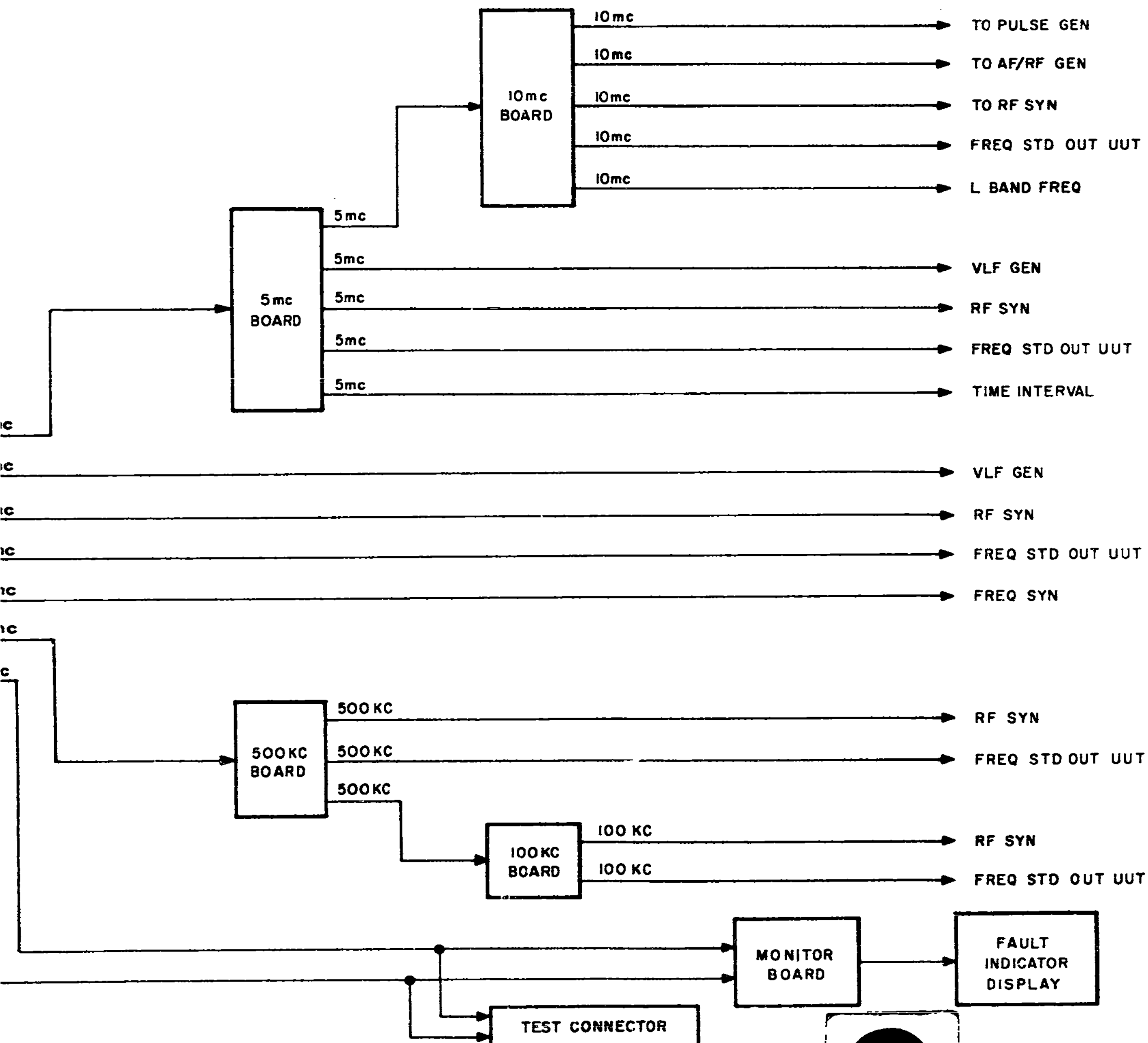


Figure 6-25. Frequency standard - block diagram

2

8. 370 to 460 Mc Phase Locked Loop

Major activity for this loop is scheduled for the coming quarter.

9. Final Mixer and Output Stage

Major activity for these items is scheduled for the coming quarter.

E. Frequency Standard

a. Progress and Status

The revised block diagram of the Frequency Standard is given in Figure 6-25. The major change is that the basic frequency is obtained from a Crystal-Controlled Standard.

The one-megacycle board has been designed, tested, and released to drafting. The voltage regulator has been designed but will not be breadboarded.

The drift rate of the Crystal Controlled Standard is less than 5 parts in 10^{10} in 24 hours and is approximately the same whether the unit is tuned on or off. In 90 days this will amount to a drift of 450 parts in 10^{10}. Variations in temperature can cause a maximum deviation of 400 parts in 10^{10} and power supply variations can cause a maximum deviation of 50 parts in 10^{10}. These add up to a total of 900 parts in 10^{10}.

Ninety days after calibration, the actual frequency is composed of two components: (1) drift and variation during the 90 days; and (2) drift during warmup. The first component is 900 parts in 10^{10}. The second component is 1 part in 10^8; see Figure 6-26 which shows that regardless of temperature at start up, the unit is within 1 part in 10^8 is less than 10 minutes. Therefore the actual frequency will be within 1000 parts in 10^{10}, or 1 part in 10^7 within 10 minutes.

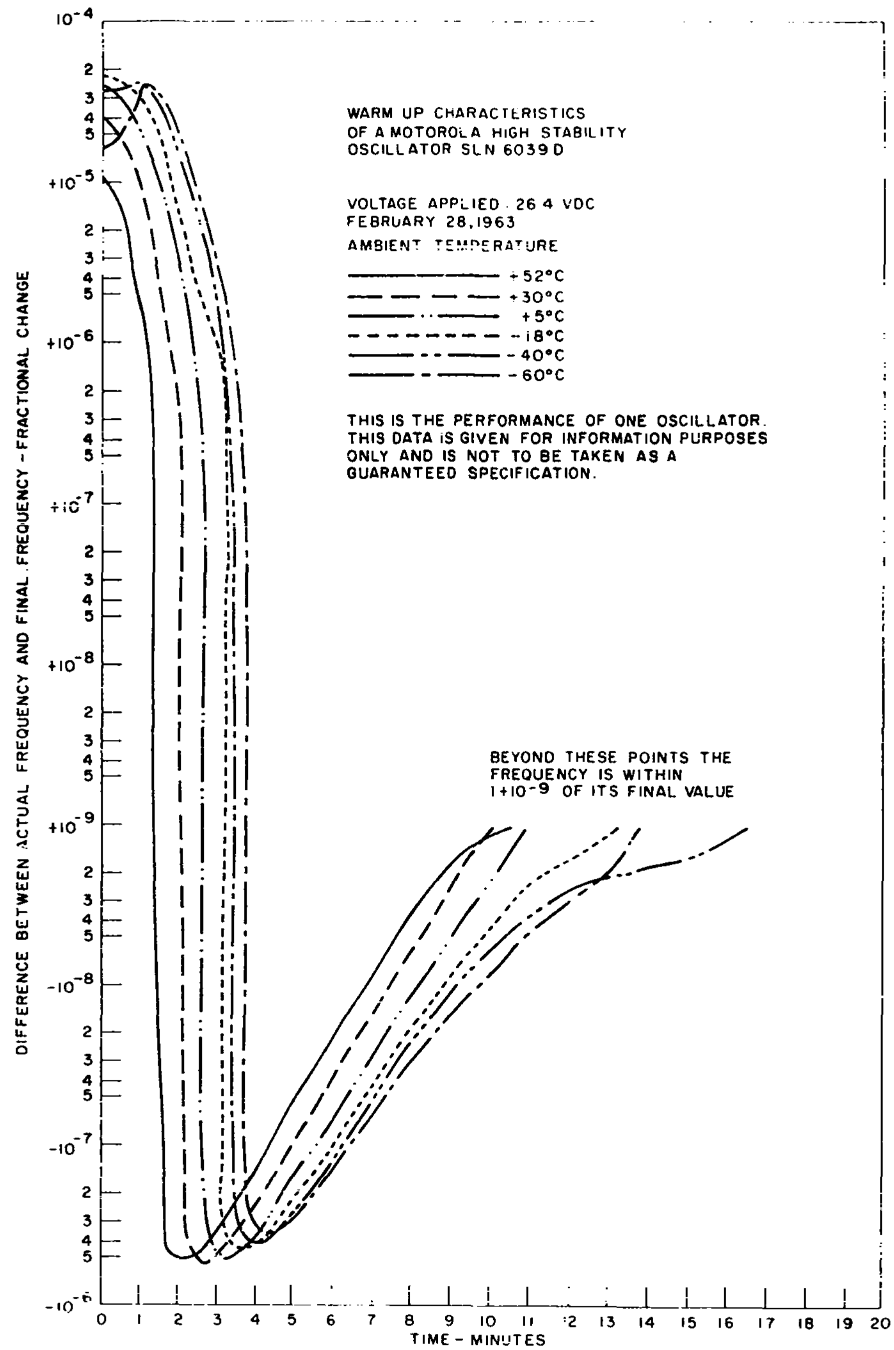


Figure 6-26. Warmup characteristics of crystal controlled standard

Allowing a safety factor of a 5-minute variation in warm-up time between different Motorola oscillators, it can be stated that the Frequency Standard will be within the allowed tolerance (1 part in 10^7) within 15 minutes after turn-on, provided recalibration occurs at 90-day intervals.

F. Output Attenuator and Level Detector

a. Progress and Status

Figure 6-27 shows this unit in block diagram form. Four changes were made in the design: (1) the number of inputs has been reduced to one; (2) a wideband amplifier has been added at the output; (3) the values of attenuation available in each decade have been changed; and (4) a squaring amplifier has been added for use with the 1-megacycle input. The latter satisfies the 1-megacycle square wave requirement.

The specification control drawing for the coaxial attenuator has been completed and has been released for procurement.

The wideband amplifier has been breadboarded, the worst case calculations have been made, and the unit has been tested over the temperature range. The unit met its specifications; however, a change in one of the transistor types was indicated. After additional temperature tests have been completed with the new transistor, the wideband amplifier will be released during the next quarter to drafting and manufacturing.

The level detector has been completed through the paper design, parts have been received, and the breadboard is about to be built and tested. The level detector will be released for manufacturing during the next quarter.

G. Pulse Generator

a. Progress and Status

Figure 6-28 is the revised logic diagram for the Pulse Generator. The revisions consisted of simplification of the circuit design and elimination of redundant

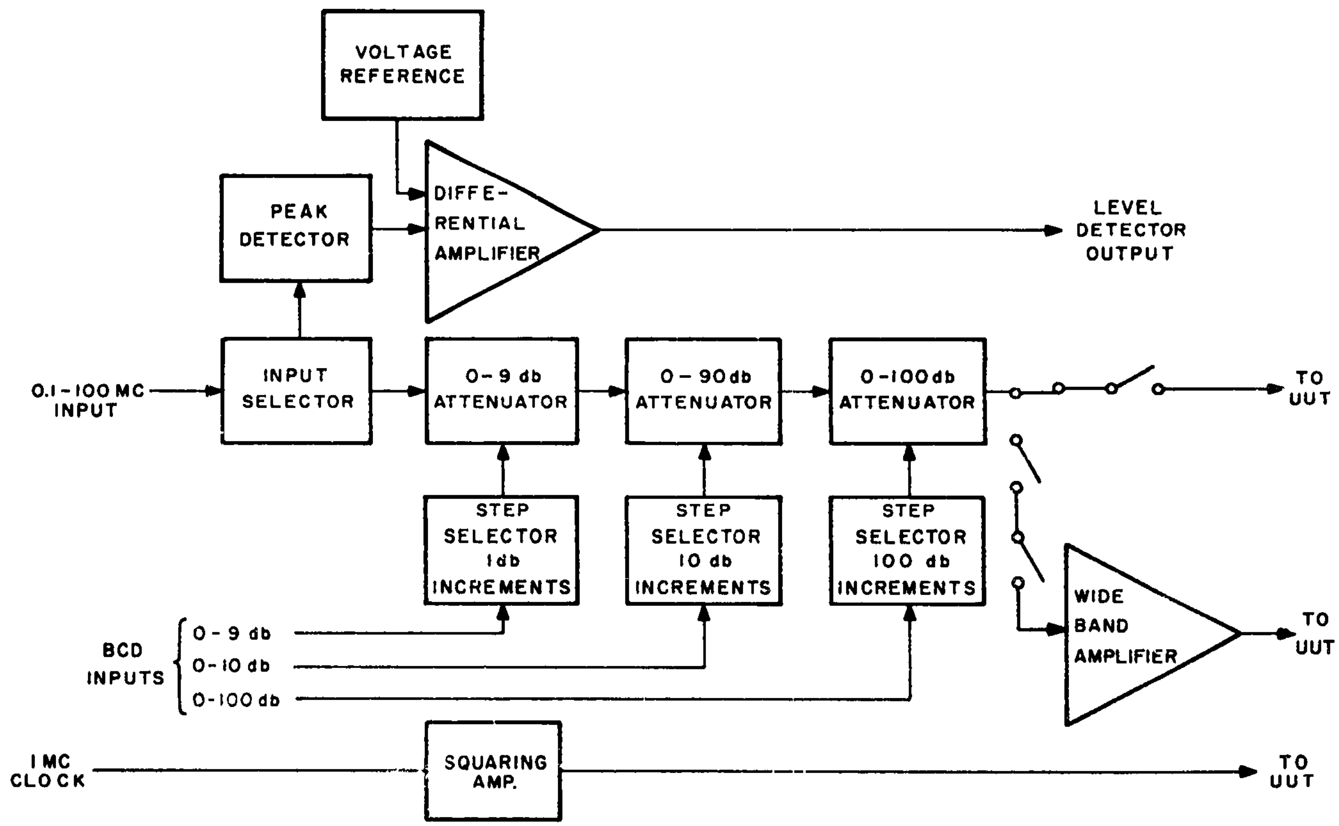


Figure 6-27. Output attenuator and level detector - block diagram

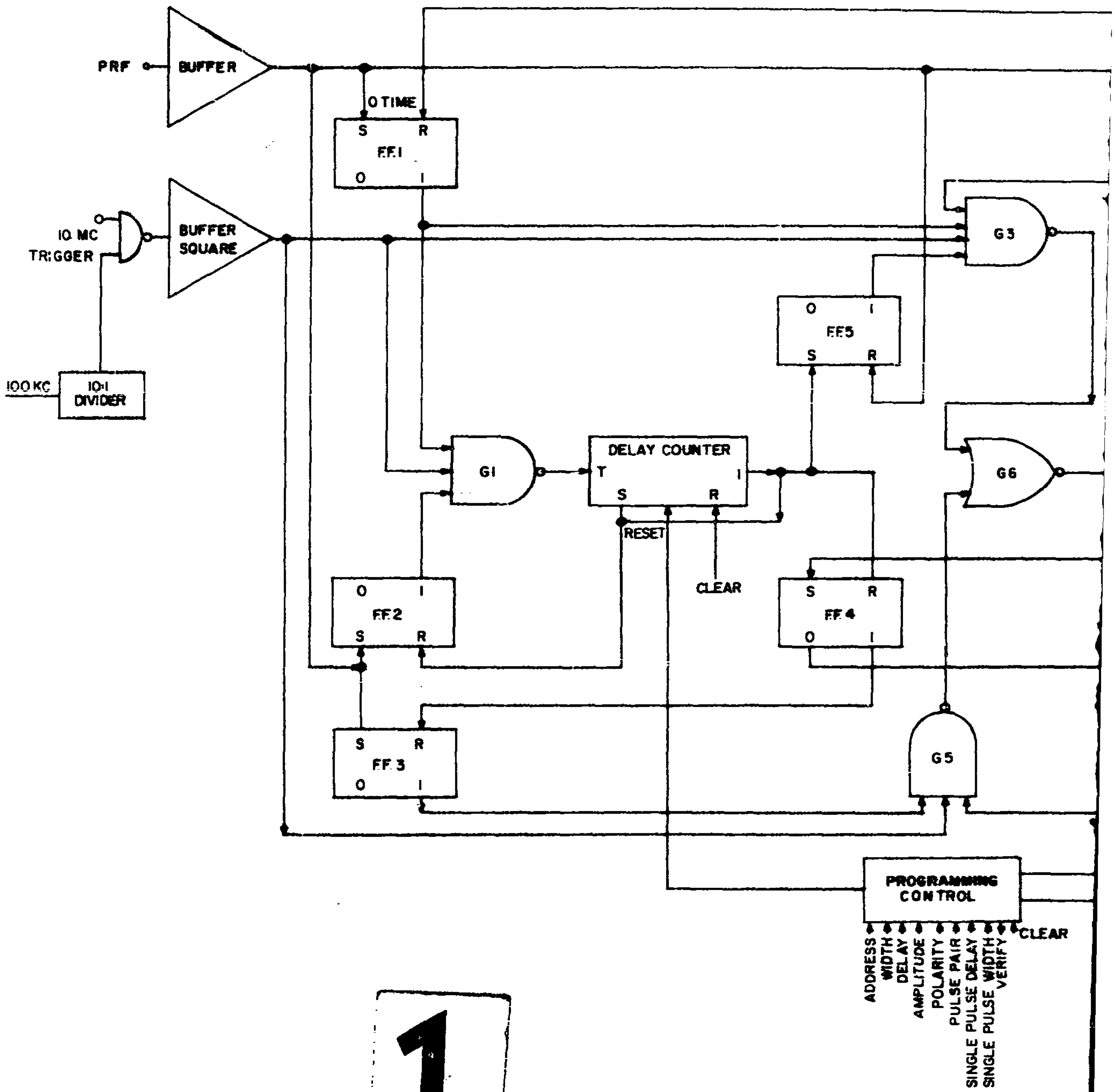


Figure 6-28. Pulse generator - logic block diag

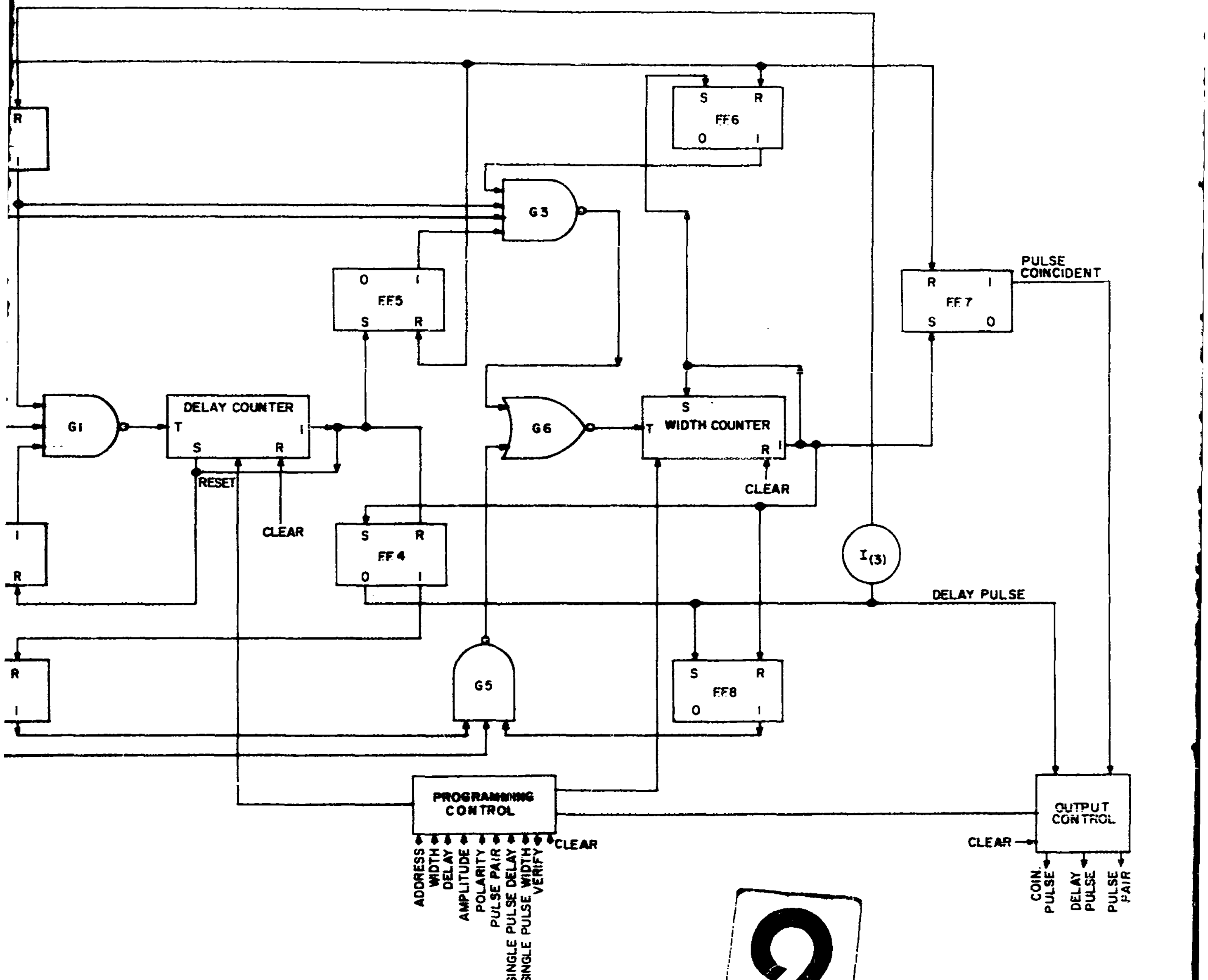


Figure 6-28. Pulse generator - logic block diagram

2

circuits. The functions performed are the same as described in the Second Quarterly Interim Technical Report. This unit satisfies the basic requirements of variable pulse width, pulse height, and variable delay between pulses. Variable repetition rate is obtained by supplying a variable frequency input from the AF/RF generator.

Figure 6-29 shows the breakdown of the unit as it has been subdivided into the various plug-in assemblies.

The Input Control shown in Figure 6-29 contains nearly all the logic shown in Figure 6-28. This function has been breadboarded and released to drafting. During the next quarter, it will be released for manufacturing.

The Trigger Selector board selects the 10-Mc input when pulse widths and pulse delays are less than 999.9 μsec; 100 kc is selected when widths and delays are greater than 999.9 μsec. Standard MTE millimodules will be used; this board will be breadboarded and released for manufacturing during the next quarter.

As indicated in Figure 6-29, the counter, comparator, and storage functions require eleven boards. The counter and storage boards are Standard MTE boards and therefore do not require design for this specific application. The comparator board is not a Standard MTE board; it was designed and released to drafting, and will be released to manufacturing during the next quarter.

The Address boards are Standard MTE boards and therefore do not require design for this specific application.

The Output Control boards, which are not Standard MTE boards, were designed. Breadboarding will not be required, except for the amplitude control portion of the output buffer; this will be accomplished during the coming quarter and these boards will be released to manufacturing.

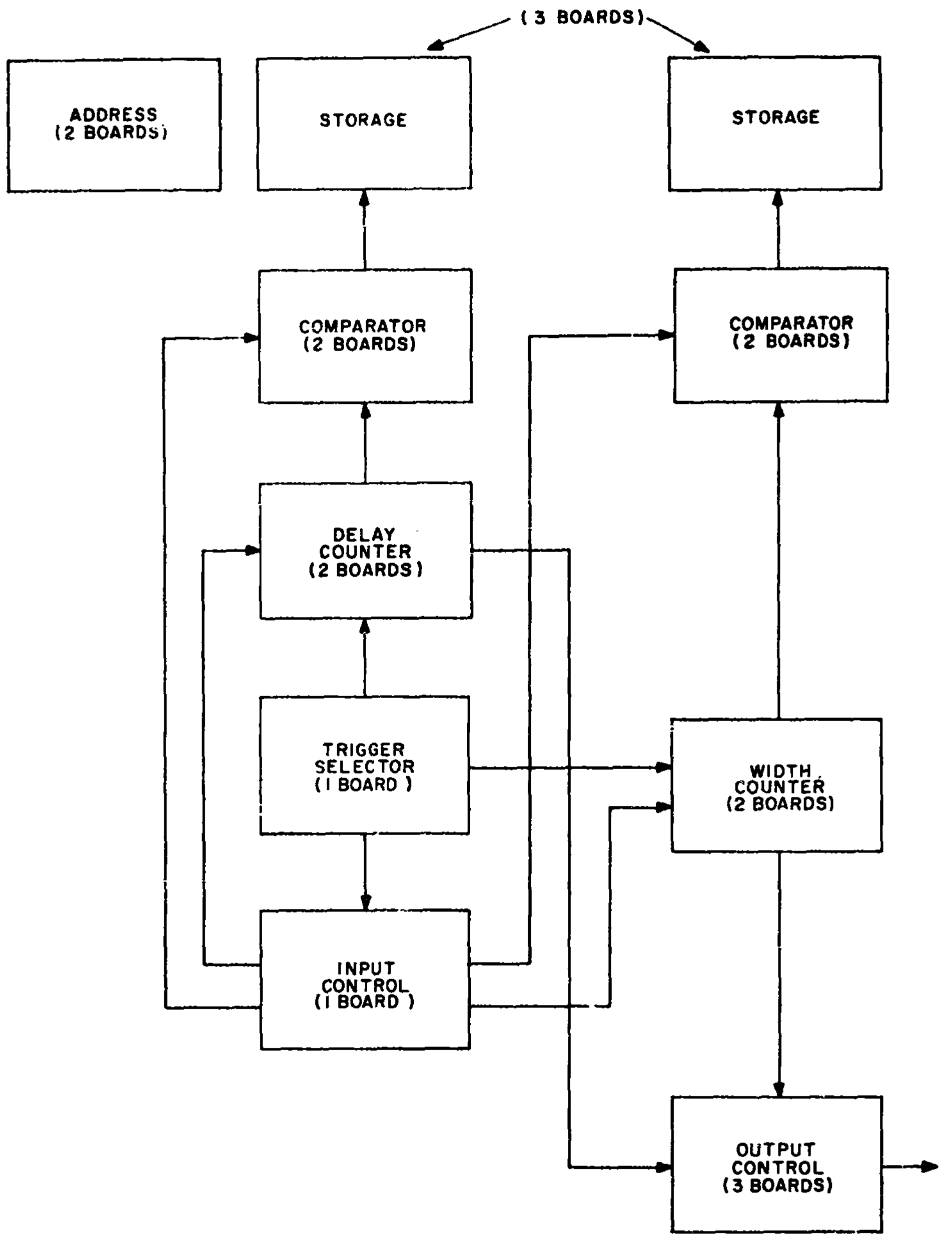


Figure 6-29. Pulse generator - breakdown of plug-in assemblies

H. Message Generator

Further examination of the Test Requirements Analysis has indicated that the characteristics previously specified for this unit will not be adequate to meet the Mauler requirements and the data available is not adequate to define the requirements. Work on this unit has been stopped pending the receipt of additional information.

I. Message Receiver

Further examination of the Test Requirements Analysis has indicated that the characteristics previously specified for this unit also will not be adequate to meet the Mauler requirements and the data available is not adequate to define the requirements. Work on this unit has been stopped pending the receipt of additional information.

J. Phase Converter and Power Amplifier

The design approach and block diagram have not changed since the previous report was published. Work on this unit will be performed during the second quarter of 1963.

K. Resistive Load

The function of the DC/AF Switching Unit has been added to the Resistive Load chassis. A parts list has been completed for the unit and a preliminary schematic has been determined. The preliminary layout of the chassis was made to ensure that both functions could be incorporated in a single chassis. This work has been completed and the change in the specification to include the function of the DC/AF switching unit in the Resistive Load is being accomplished. The relay driver circuits were breadboarded and tested. The schematics and specification control drawings for all parts included in this unit have been completed and released to manufacturing. The layout for the chassis will be completed during the next quarter and released to manufacturing.

L. 400 cps Power Supply

A circuit was developed for this power supply. It includes a filter in the SCR control circuitry to eliminate the amplitude jitter noted in the previous elementary circuits. Construction of a breadboard began, covering one phase of this three-phase supply. During the next quarter, breadboard activity will be completed, and the power supply will be released to manufacturing.

M. 800 cps Power Supply

The output current requirements for this supply have been changed from three amperes per phase to one ampere per phase. This is based upon a re-examination of the Mauler Test Requirements. The design of this unit will be started and completed during the coming quarter. This power supply will use essentially the same circuit as the 400-cps power supply.

N. Circuit Breaker Disconnect Unit

The electrical schematic and mechanical design have been completed, and the front panel layout has been submitted for approval. The component parts with the exception of the front panel have all been released for manufacturing.

O. 115/10 Volt AC Power Supply

This power supply, required for the Hydraulic Test Group, furnishes 400-cps single-phase stimulus power programmable to either 115 or 10 volts at rated full load current of 1 ampere. The mechanical and electrical design were completed. This supply will be released for manufacturing, during the next quarter.

P. Low Frequency Stimulus Routing Assembly

This is a new unit which has been added since the previous reporting period. Its function is to route signals between various assemblies in the Low Frequency Stimulus and from the Low Frequency Stimulus to other MTE subsystems. The unit requires one full-width 7-inch high chassis. A schematic of the unit is shown in Figure 6-30. As indicated, the unit consists of a group of relay trees

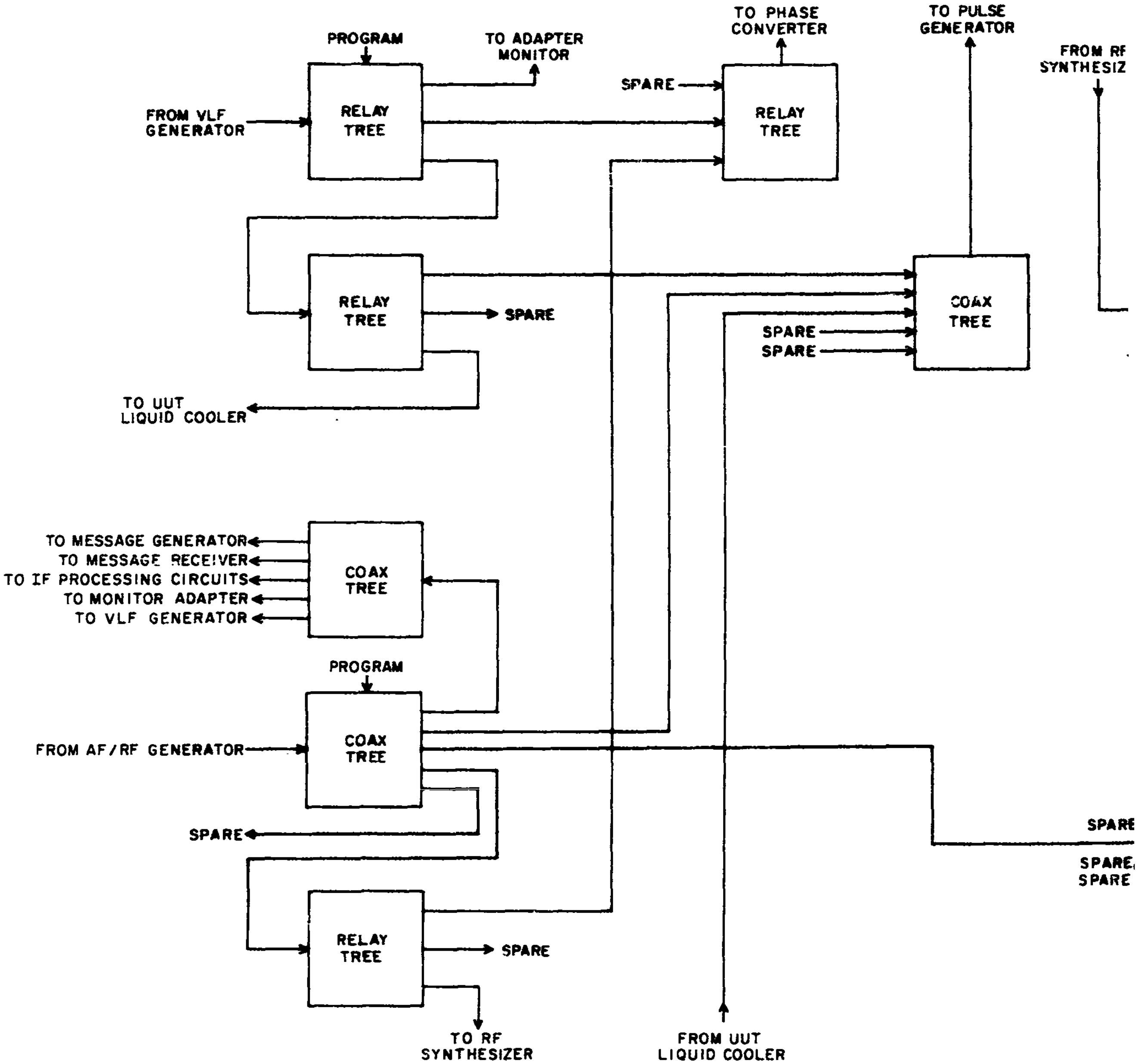


Figure 6-30. Stimulus routing - simplified block diagran

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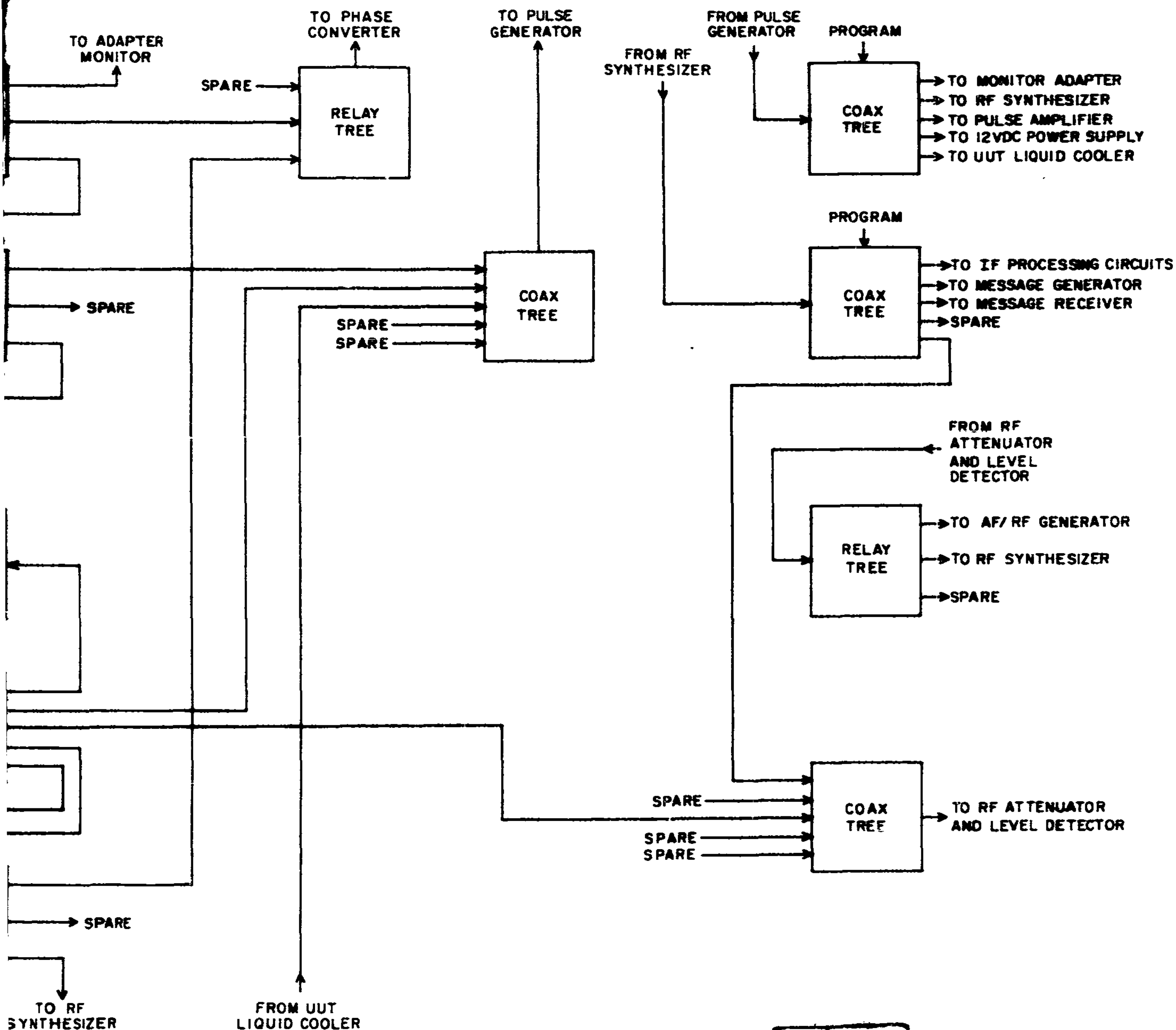

Figure 6-30. Stimulus routing - simplified block diagram

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commanded by the program controller. A preliminary selection of the components to be used has been made and the unit is undergoing layout. This unit does not require a breadboard; it will be released for manufacturing during the next quarter

Q. Mauler Synchronizer

The Mauler Synchronizer MTE 5896 was added to the complement of Low Frequency Stimulus generators during this quarter to supply Mauler peculiar pulse requirements. As shown in the preliminary block diagram, Figure 6-31, the Mauler Acquisition Radar Synchronizer unit forms a basic part of this new unit. The other elements shown will provide programming data and synchronizing pulses to be used to simulate a radar return.

Detailed design of this unit is scheduled to begin and be completed during the next quarter. Breadboarding and release to drafting will be accomplished during the next quarter.

6.1.5 DC STIMULUS

A. 0 to 9.99 Volt DC Stimulus

Design of the relay-controlled programmable resistor network was completed. See Figure 6-32, which shows a DACON with an internal impedance of approximately 5 ohms. To achieve the desired accuracy, the contact resistance variation of normal metallic-contact relays must be bettered by a factor of at least 10. Therefore mercury-wetted relays are presently designated for this use. The disadvantage of this type of relay is the restricted mounting position; the maximum allowable tilt from vertical is 30 degrees. This limitation is not judged to be serious. The alternative to the foregoing design would be a higher impedance DACON (say, 100 ohms or more) followed by a gain-of-one operational amplifier; this approach is not as attractive because of greater complexity, lower MTBF, and possible additional sources of error.

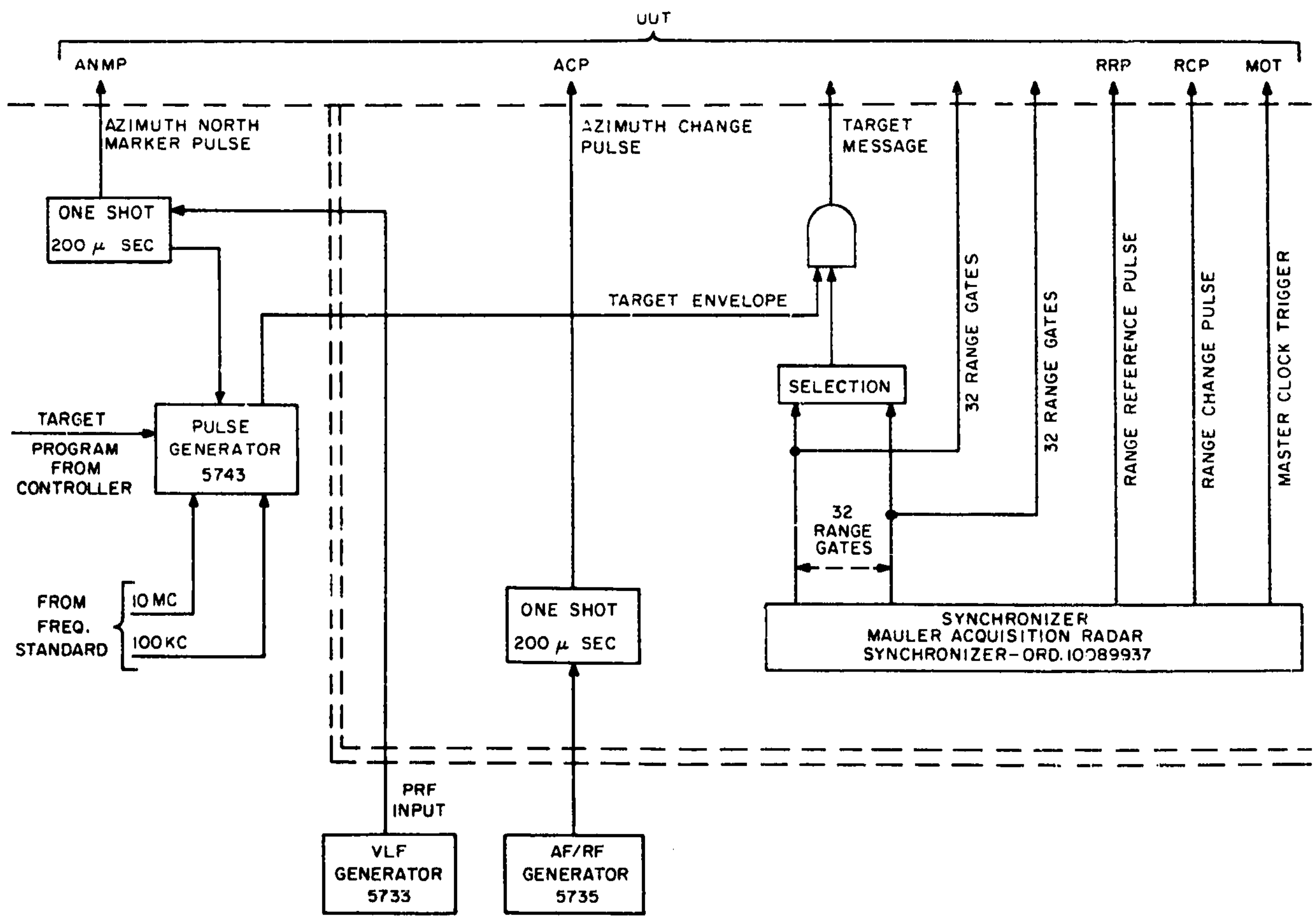


Figure 6-31. Mauler synchronizer - simplified block diagram

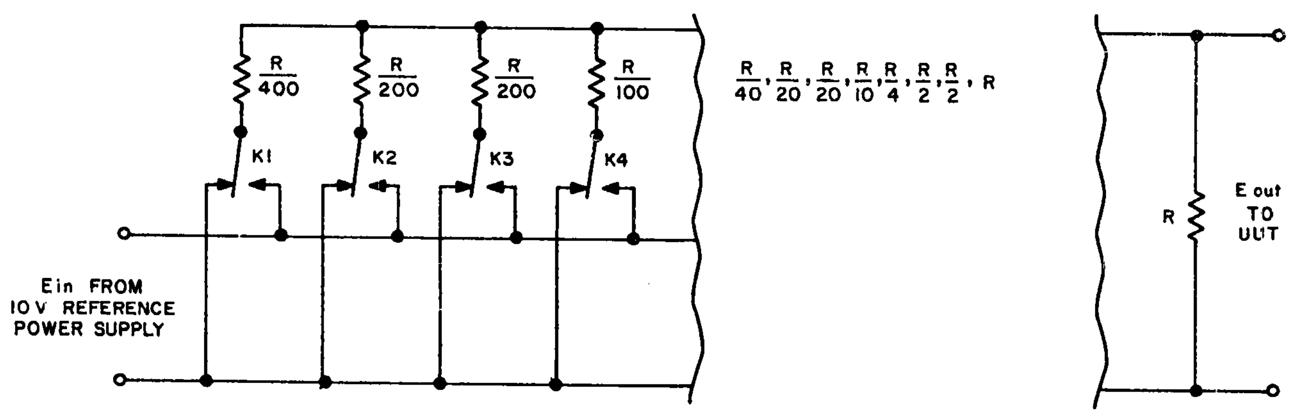


Figure 6-32. 0-9.99 vdc stimulus - programmable output voltage network

The DACON operation requires a 1-2-2-4 BCD code, whereas the input programmed code will be 1-2-4-8. Conversion between codes is accomplished using Standard MTE relay driver circuits. See Figure 6-33.

Any quantity of DACONs from one to three, with the associated 10 volt DC reference power supply, can be accommodated in one 7-inch rack unit using the single 10-volt reference supply. The output voltage level of the DACONs may be independently programmed. However, because all DACONs use the same supply the polarity must be the same for each DACON.

No further design or breadboard work is required on this stimulus.

Release of parts has begun. This will continue through the next quarter, and be completed during the third quarter of 1963.

B. 0 to 36 Volt DC Stimulus

The first circuit design was based on a 0 to 36 volt stimulus unit with the output programmable in 1-volt steps and a 10-amp capacity. The circuit was that of Figure 6-34. The compensation network was yet to be determined. The circuit was breadboarded for three reasons: (1) to evaluate the pass transistor heat sink; (2) to check the operation as compared to the theory; and (3) to check the operation of the two-loop control system which appeared to be required.

The tests of the heat sink were made with the pass transistor isolated from the heat sink by means of mica washers. Silicone grease was used to improve heat transfer. Temperature measurements were taken on the transistor base, transistor stud, and heat sink next to the transistor. These measurements revealed that the thermal impedance of the mica washer was too great and the full capability of the transistor could not be realized. Removal of the mica washers solved this problem and the heat sink proved to be adequate.

A check of the circuit for ripple showed that the circuit was oscillating and compensation was needed.

FOR VOLTAGE RATIO	EVOLUTION OF DACON CODE THROW RELAYS	RLATIVE WEIGHT
0.1	K4	1
0.2	K3	2
0.3	K4 AND K3	1+2
0.4	K1	4
0.5	K1,K4	4+1
0.6	K1,K3	4+2
0.7	K1,K3,K4	4+2+1
0.8	K1,K2,K3	4+2+2
0.9	K1, K2,K3,K4	4+2+2+1

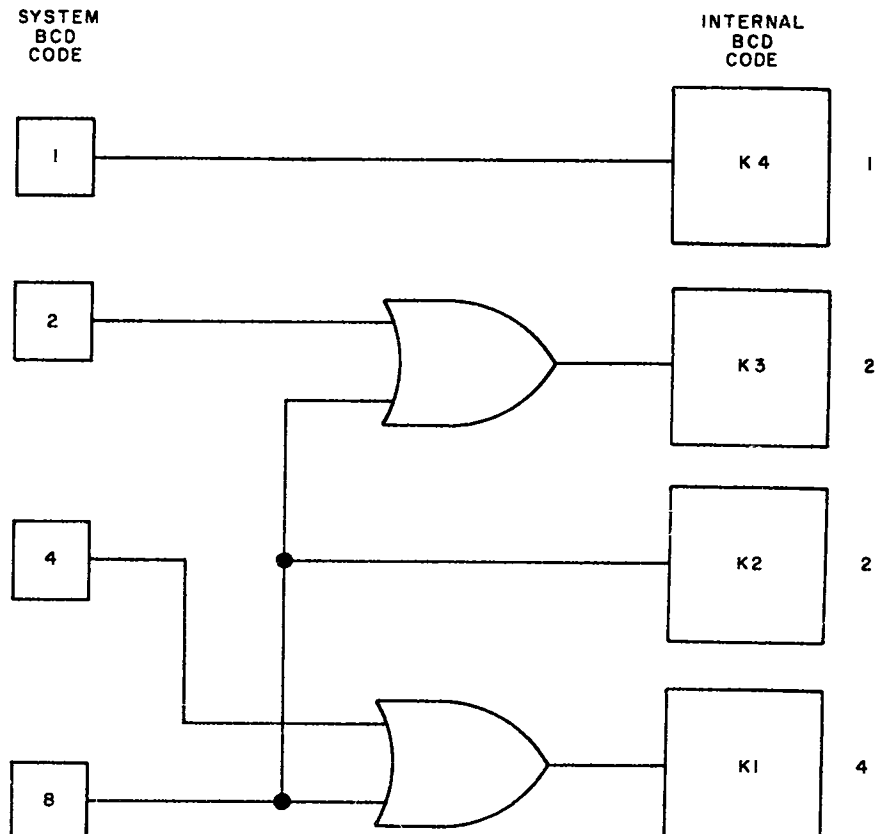


Figure 6-33. 0-9.99 vdc stimulus - code conversion system

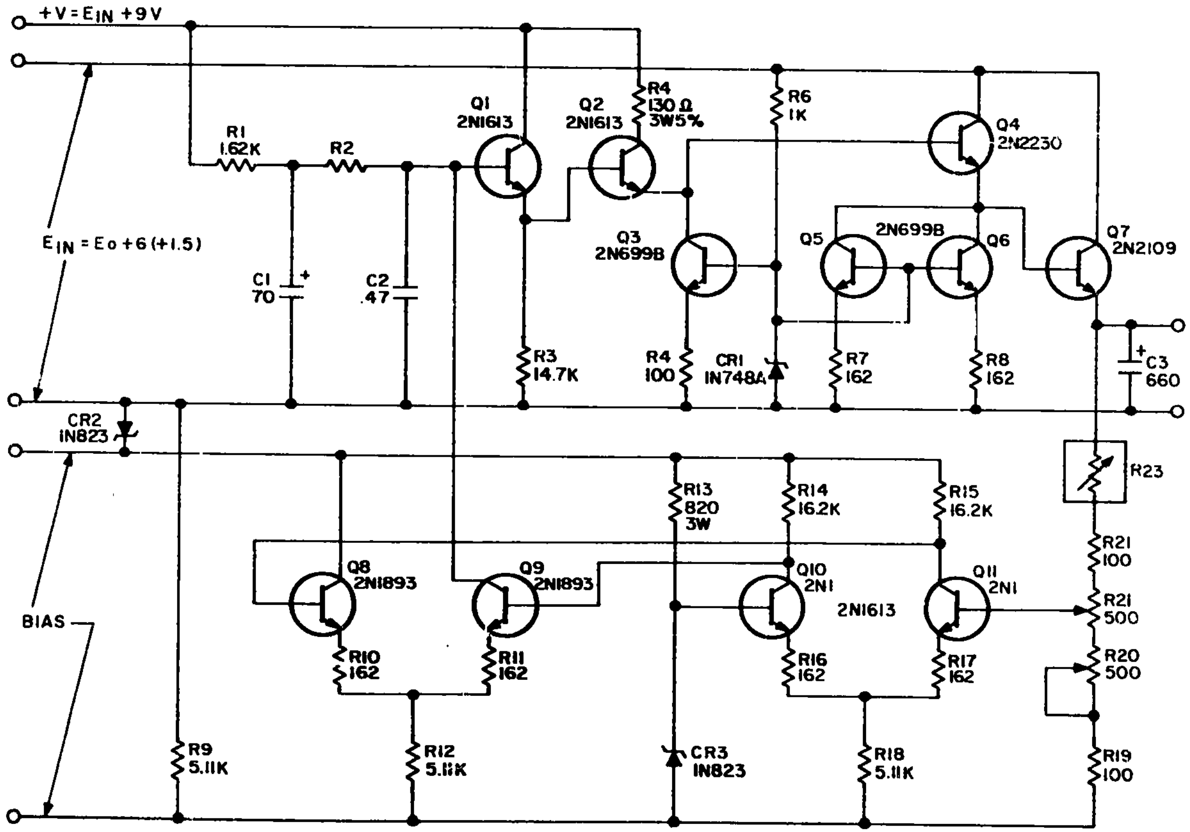


Figure 6-34. First circuit design 5-36 vdc stimulus programmable regulator

A temporary compensation network was added to stop the oscillation so that regulation tests could be made. The regulation tests showed that the gain was satisfactory.

Subsequently a review of the TRA was made with the result that the output current requirement was increased from 10 amperes to 20 amperes. The increased current capacity made a redesign necessary. Theoretical analysis showed that better preregulation of the input voltage to the main regulator would be necessary to prevent overdissipation in the pass transistor. More gain would be required to obtain the desired regulation. The redesign resulted in the circuit shown in Figure 6-35. The buffers Q6 and Q9 were necessary to prevent effects of loading. The programmable bleeder was necessary to keep the beta of the pass transistor from falling off and to provide a discharge path for the output capacitor. R6 was added to reduce the power dissipation in the pass transistor. This circuit still did not have sufficient gain because the load resistor for Q8 was small. The size of this resistor was dictated by the input voltage which in turn had to be kept at E_{out} + 6 volts, approximately, to minimize power dissipation in the pass transistor and driver.

This problem was solved by returning R1 and Q1 and Q2 collectors to a bias voltage which is kept 9 volts above the output. The resulting circuit was satisfactory from an operational point of view but the total power dissipation of 740 watts was greater than could be tolerated.

Further design effort was necessary to reduce overall power dissipation. Large amounts of power were dissipated in R4 and R5 of Figure 6-35 when the output voltage was programmed to higher values. The solution was the replacement of fixed resistors with constant current sources. The new circuit is shown in Figure 6-36. Q3 and Q5 are the constant current loads for Q2 and Q4. R2 and C2, R9 and C4, R15 and C5 form the necessary compensation networks to prevent the circuit from oscillating. This circuit dissipates approximately 175 watts less than the original circuit.

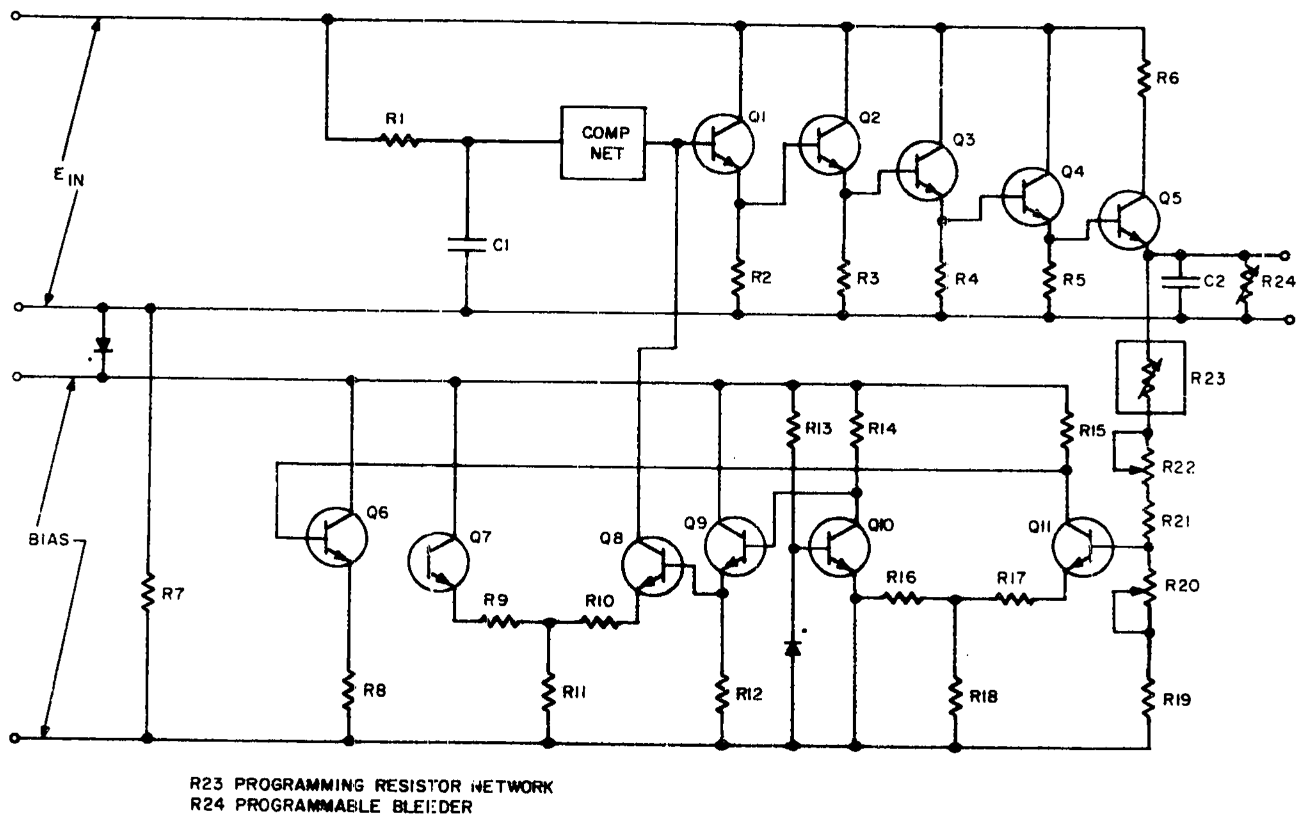
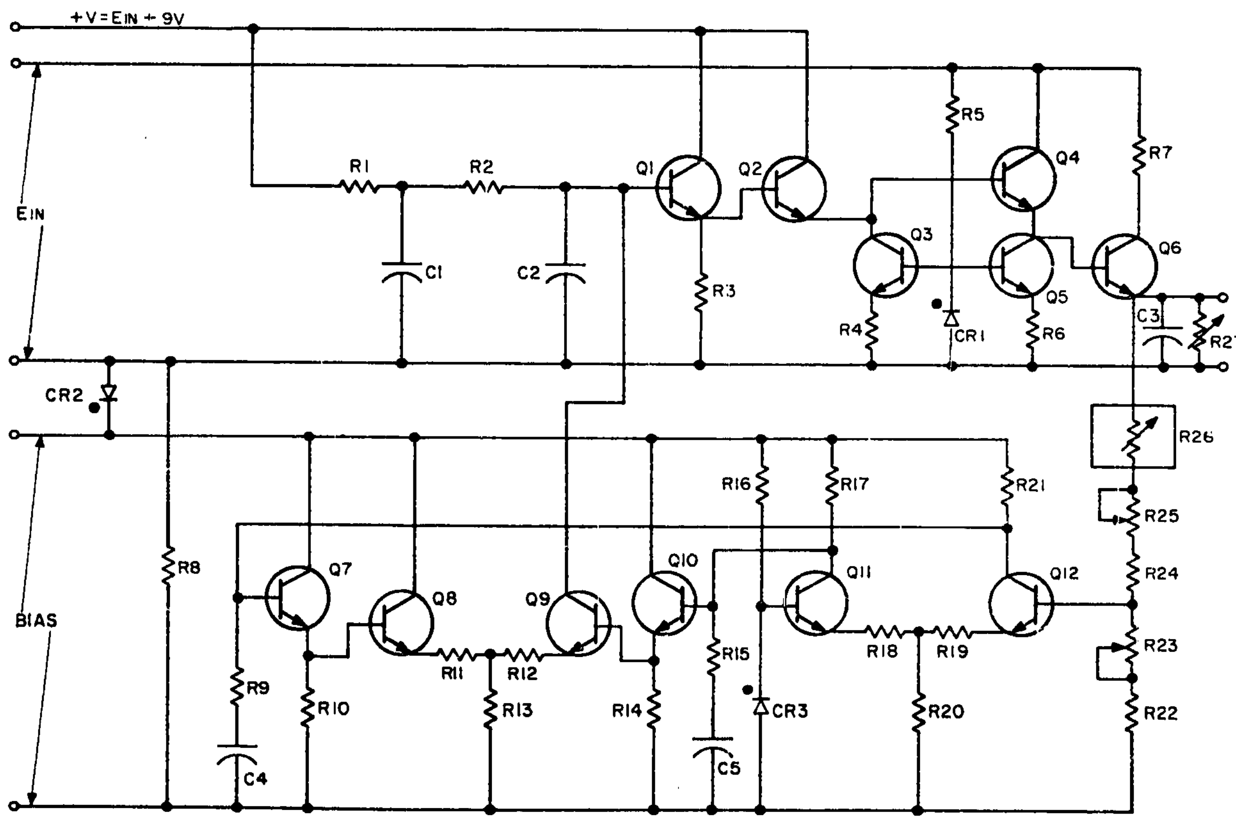


Figure 6-35. Redesigned 5-36 vdc stimulus circuit programmable regulator



R26 PROGRAMMING RESISTOR NETWORK
R27 PROGRAMMABLE BLEEDER

Figure 6-36. Final circuit design 5-36 vdc stimulus programmable regulator

The 9 volt bias supply has been designed. The circuit consists of a 3 phase full wave bridge driving a conventional electronic regulator. This supply must be very stable, for a change in its voltage can appear as an error in the output voltage.

The 16 volt bias supply which drives the emitter followers is not as critical as the 9 volt bias supply as far as regulation is concerned. Low ripple and noise are required to keep output ripple and noise at the desired level. This supply consists of a 3 phase full wave bridge driving an RC filter and a zener regulator.

A preliminary circuit for an SCR preregulator has been designed and built. The results are discussed in the following subsection, High Voltage Stimuli. The overall loop consisting of regulator and preregulator has not yet been closed.

Design of the programmable voltage output network (R26) was completed. It is essentially the same as the 0 - 9.99 volt stimulus except that code conversion is not required.

Preliminary chassis layout of the complete unit was finished. Schematics and printed board layouts were released to drafting. Parts release began.

During the next quarter, breadboard tests will be completed, and release for manufacturing will be made.

C. High Voltage DC Stimuli

a. Progress and Status

This section covers the 20 to 30 volt DC Stimulus and the 280-850 volt DC Stimulus; the design approach on each of these is essentially the same. See Figure 6-37. For discussion purposes, the design is separated into four subjects - programming, rectifier section, series regulator, and preregulator.

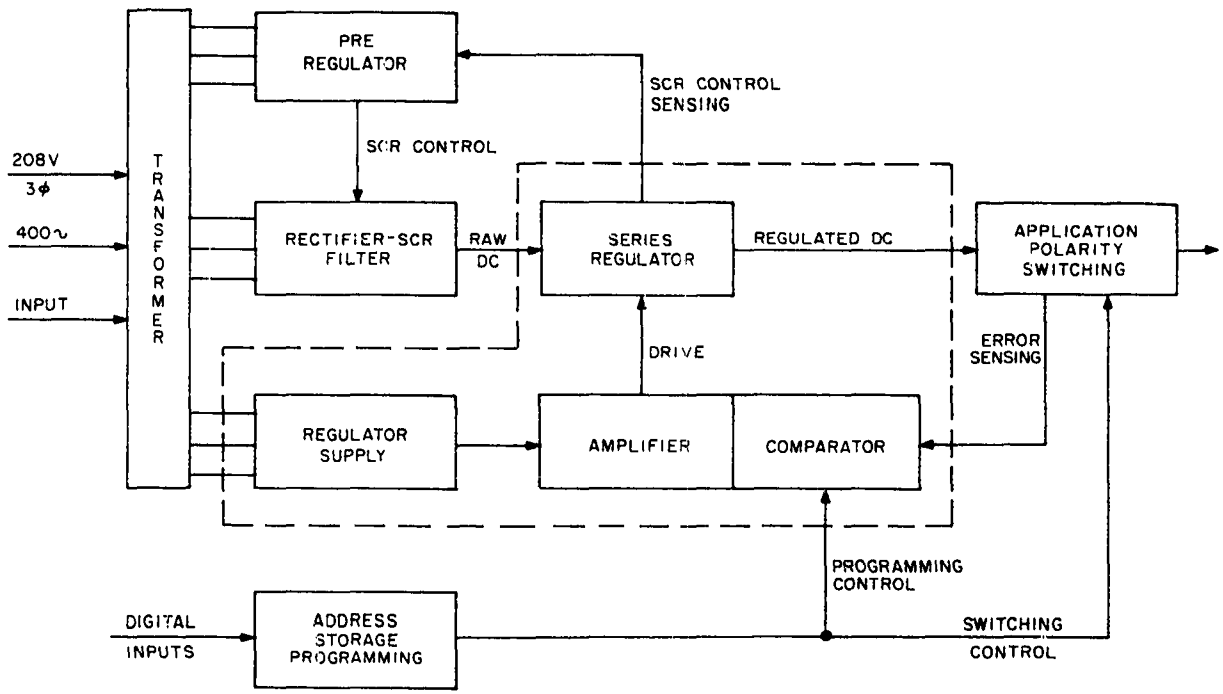


Figure 6-37. High voltage stimulus - block diagram

1. Programming

The conventional method of programming the output voltage (see Figure 6-38) by varying one leg of a voltage divider across the output resulted in a more complex design than desirable, since one bit had to be subtracted from the programmed value before one-for-one application to the programming relays. The alternate "potentiometric sensing" method (see Figure 6-39) was employed, eliminating this undesirable condition and allowing simple one-for-one relay operation without the need for decoding the BCD input data.

The application switches and programming switches are operating under a severe voltage and current stress since they are connected in series with and across the stimulus output. This electrical stress is greater than the standard relay can withstand, therefore specifications for a relay to meet these requirements have been generated and samples of relays built to handle these stresses are under evaluation. Based on the results to date, a selection has been made; however, tests will continue to determine adequacy of the relays over a long period of operation.

2. Rectifier Section

It was found that, under conditions of light load, insufficient current flowed through the SCRs to keep them in the conducting state during the line cycle, therefore an erratic output voltage was obtained. A dummy load on the series regulator output (see Figure 6-37) would not correct this condition, since the filter effectively decoupled the load current from the instantaneous rectifier current. A dummy load, composed of several resistors having a value that is switched with the programmed output, was designed to be placed across the rectifier output. This "quasi-constant-current" circuit has been breadboarded and tested, and satisfactorily corrects the original condition.

3. Series Regulator

Another effect of light load operation was fall-off of beta of the series regulator transistor. This caused the output impedance to rise above specification limits. Another "quasi-constant-current" dummy load circuit was designed,

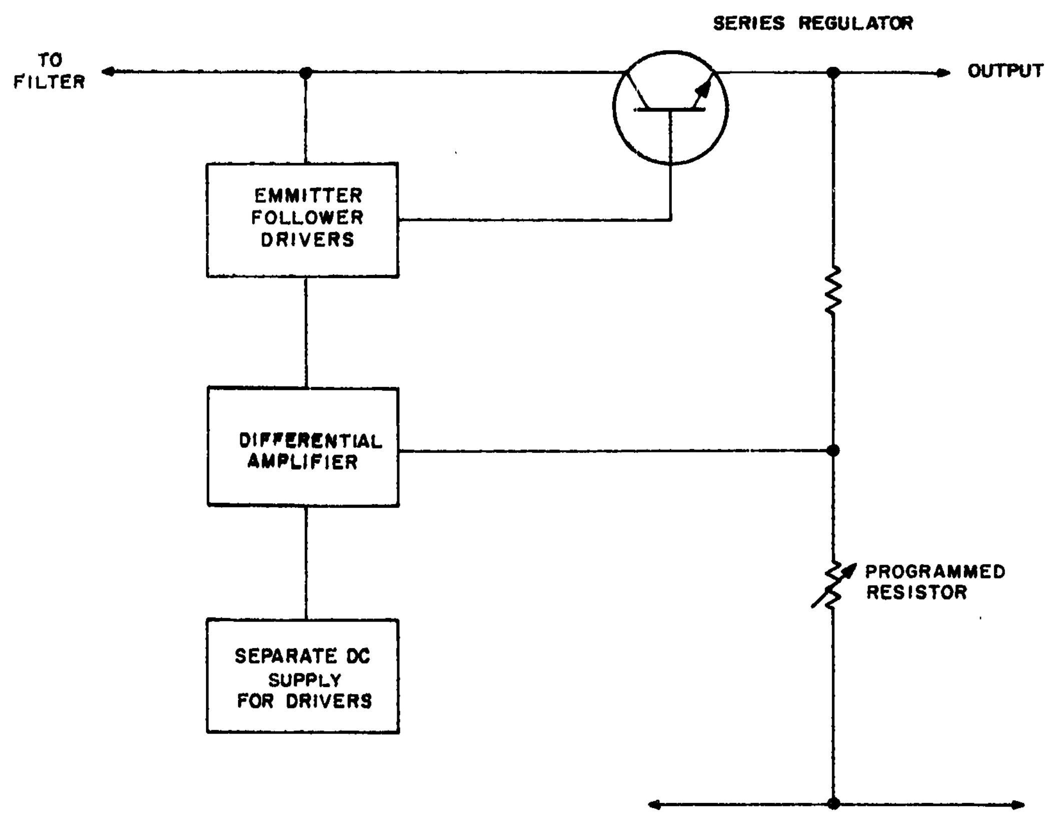


Figure 6-38. High voltage stimulus - conventional programming of output

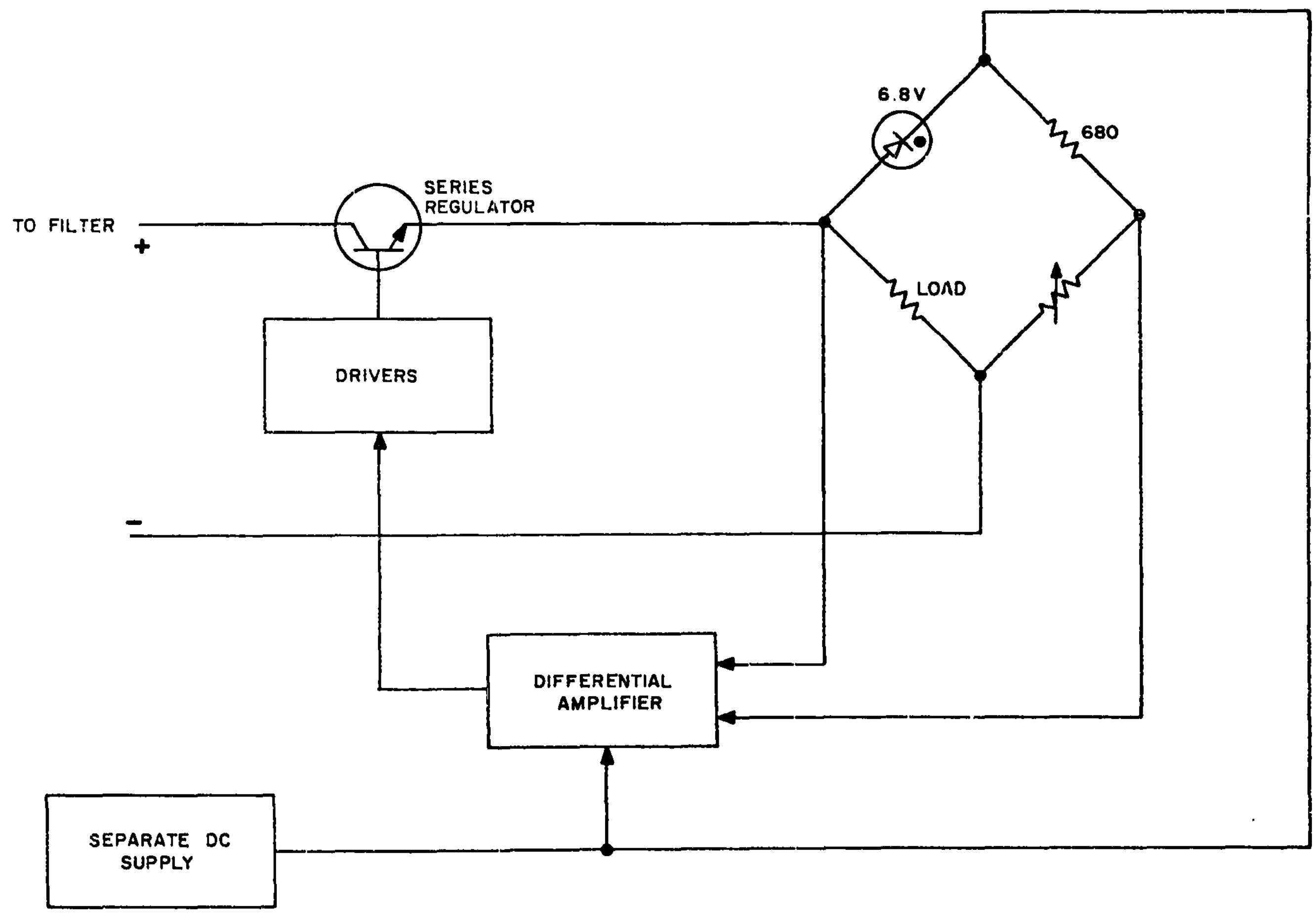


Figure 6-39. High voltage stimulus - potentiometric programming of output

similar to the one discussed above, and similarly switched with the programming. This circuit has also been breadboarded and tested, and proved satisfactory.

4. Preregulator (Trigger Circuit)

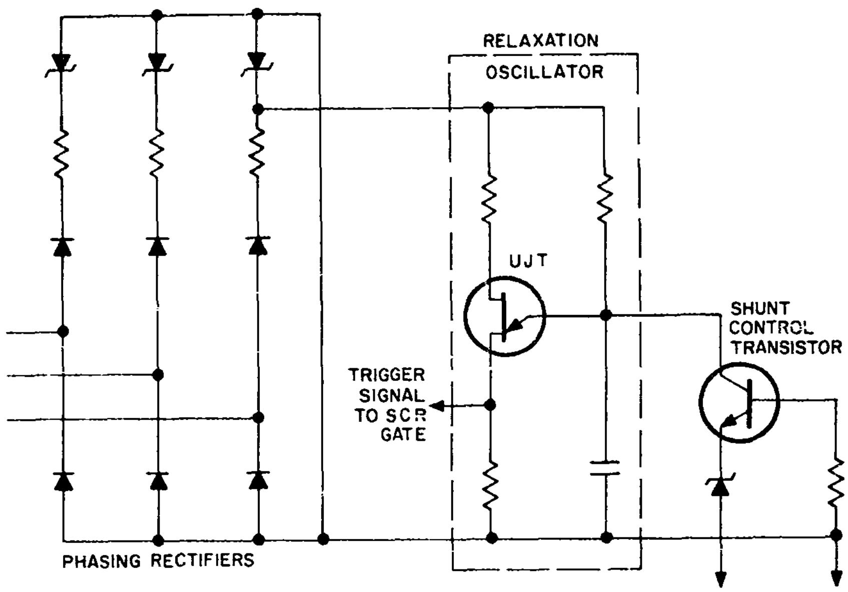
Two types of SCR Trigger Circuits have been designed and laboratory models have proven feasible. See Figure 6-40. The conduction angle for the SCRs is controlled by the timing of pulses from unijunction transistor relaxation oscillators; pulse timing is determined by an RC time constant. This time constant is varied by shunt control in the first circuit and by series control in the second. Both circuits sense voltage drop across the pass transistor and adjust the firing angle so that this voltage drop remains at a nearly constant value for all programmed outputs.

To withstand the high peak inverse voltages in the 280-850 volt DC Stimulus three SCRs are connected in series in each leg. Simultaneous triggering of the three SCRs is therefore mandatory. A special transformer has been used to perform this function, but this transformer requires considerable space, has a long lead time, and is relatively high is cost. Further work on this trigger circuit will be performed to adapt it for use with standard pulse transformers. The choice of which of the two trigger circuits to use will be made after evaluation of the complete circuit with feedback loops closed.

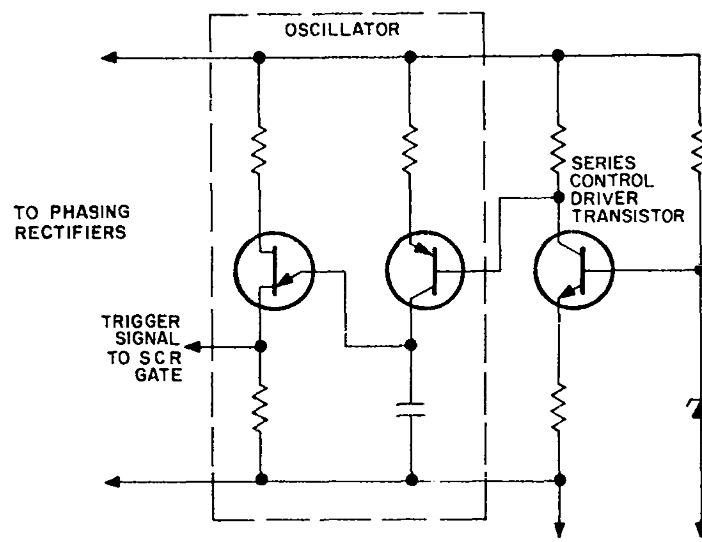
The stability of the complete circuit with its two feedback loops has been the subject of considerable study and test. Several unstable operating conditions were noted. The general principle of a much lower bandwidth in the preregulator (overall) loop would solve this problem, but the best method of achieving this lower bandwidth remains to be determined. Phase shift of the L-C filter circuit is also a current problem. Further work in these two areas will be accomplished during the next quarter.

b. Plans

(1) Breadboard tests of both high voltage stimuli units will be completed.



(A) SHUNT CONTROL



(B) SERIES CONTROL

Figure 6-40. SCR trigger circuits

(2) All drafting for the two units will be completed.

(3) The two units will be released for manufacturing.

6.1.6 MEASUREMENTS

A. Measurements Group

Circuit design of units associated with this group was completed during this report period except for possible changes to be incorporated as a result of design reviews and tests. Three printed circuit boards remain to be released to drafting. Most of the millimodules for this group have been released for manufacturing.

Figure 6-41 shows a simplified block diagram of the Measurements Group. This diagram, in addition to others included in the following paragraphs, is reproduced from the Second and Third Quarterly Interim Technical Reports to provide ready reference for the discussions that follow on the sub-units of the Measurements Group.

During the next quarter, the three remaining printed circuit boards will be released to drafting and manufacturing. The remaining millimodules will be released to manufacturing.

B. Measurement Standards

a. Progress and Status

With adoption of revisions in measurement standards specifications during this period, purchase orders were sent to prospective vendors for requote on AC and DC Voltage and Resistance Standards. Mechanical design of the standards assembly is to be based on receipt of pertinent dimensions from the selected vendors.

b. Plans

During the next quarter the unit will be finalized and placed on order.

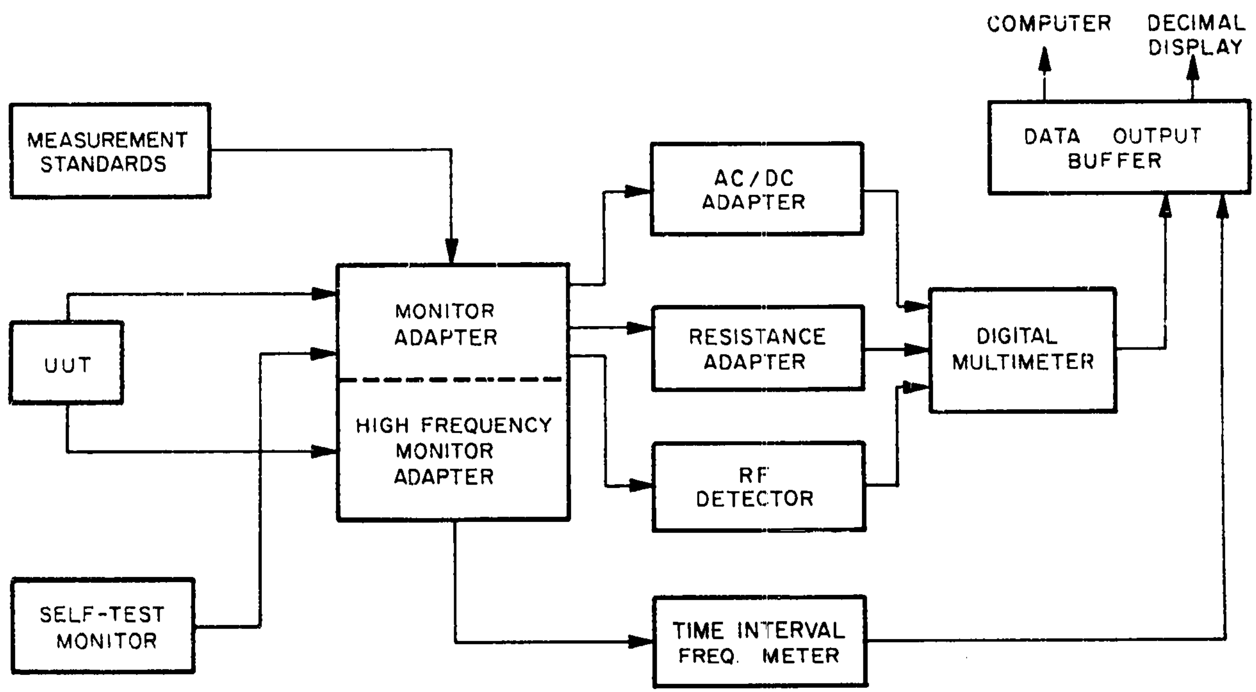


Figure 6-41. Measurements group - simplified block diagram

C. Monitor Adapter

a. Progress and Status

The design of the Monitor Adapter unit was changed to remove the UUT connectors from the front panel and to relocate them on a panel of the Control Console. Three levels of the Monitor Adapter and Self-Test Monitor were also relocated to the Control Console to minimize connection problems associated with the removal of the connectors.

All Monitor Adapter circuits were completed and released to drafting. Photomasters are complete on all six printed circuit boards, and assembly drawings are complete on four of the six.

Wiring diagrams are being drawn, and mechanical design is continuing on all chassis of this unit.

b. Plans

(1) Drawings will be completed.
(2) The Monitor Adapter will be released for manufacturing.

D. Self-Test Monitor

a. Progress and Status

Since the circuits used are identical to those of the Monitor Adapter, status and progress correspond to those of the Monitor Adapter.

b. Plans

The Self-Test Monitor will be completed and released for manufacturing.

E. Time Interval Frequency Meter (Figure 6-42)

a. Progress and Status

During the previous quarter, the following circuits were completed and the circuits released to drafting:

(1) Schmitt Trigger
(2) Start-Stop Control
(3) Input Gating Control
(4) Clock Pulse Amplifier

During this quarter, design of the decade divider drive circuits was completed and testing was begun. Specification control drawings were completed for the clock and input amplifiers and were released for equipment procurement. The decade divider and driver circuits remain to be tested and released for drafting.

b. Plans

(1) All circuit testing will be completed.
(2) All design will be completed and released for manufacturing.

F. RF Detector

Work was stopped on this detector circuit pending decision as to whether it will be built into the equipment or designed as a probe with an external cable. This decision should be made and work resumed during the next quarter.

G. AC/DC Adapter

a. Progress and Status

Final specifications for the AC/DC Adapter were prepared during this quarter and proposals from three prospective vendors were evaluated on the basis of technical approach. Price evaluation will be made prior to final choice of vendor.

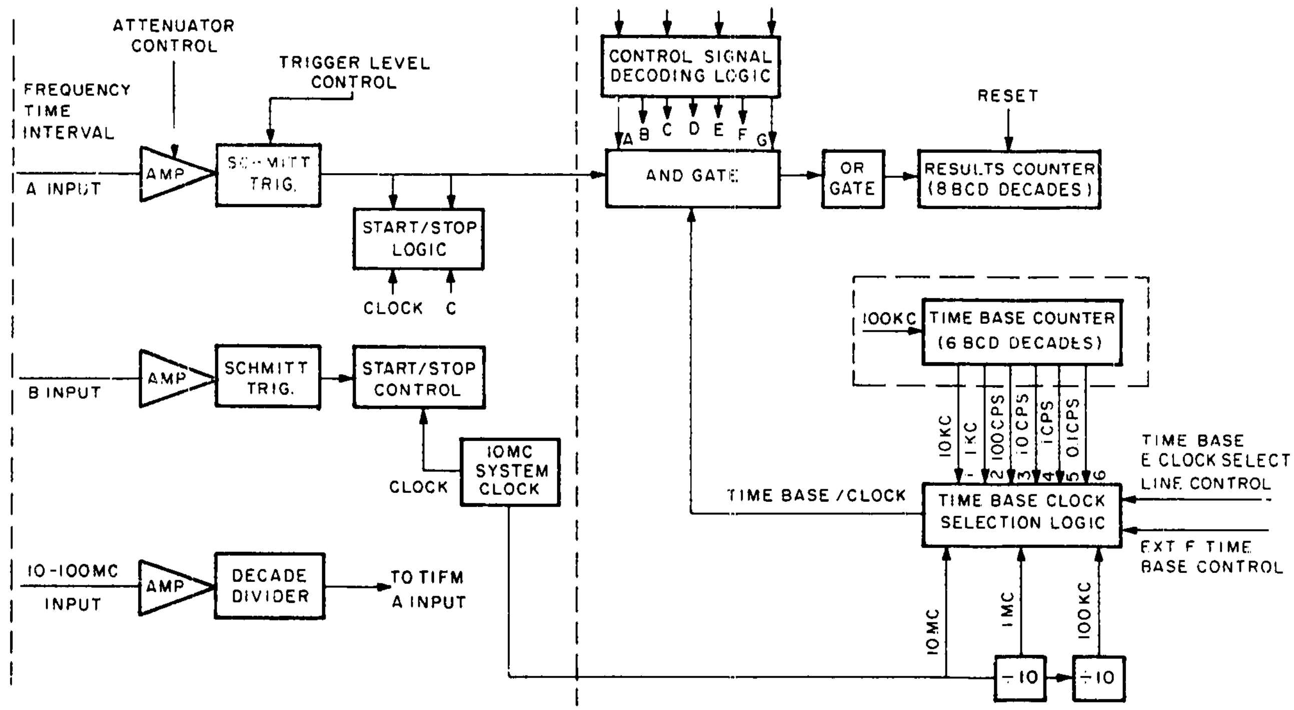


Figure 6-42. Time interval frequency meter

b. Plans

Detail design of this assembly will begin.

H. Resistance Adapter

a. Status and Progress

Components are identical to those required for the AC/DC Adapter. Decisions pertinent to the AC/DC Adapter will similarly apply to the Resistance Adapter.

b. Plans

Detail design will begin.

I. Digital Multimeter

a. Progress and Status

Effort was expended on the special circuits shown cross-hatched on the block diagram of Figure 6-43. (Refer to the Second Quarterly Interim Technical Report for details of the Digital Multimeter.) All circuits were completed and tested under room conditions with satisfactory results.

The chopper input circuit shown schematically in Figure F-1 of Appendix F was completed and released to drafting. (Operation of this unique circuit is described in Appendix F.)

This circuit has been breadboarded and is presently undergoing stability tests. Tests to date have been satisfactory.

The reference voltage system for the DECON Network was completed. The final model is undergoing regulation and stability tests.

DACON current switching requirements were established according to criteria outlined in Appendix G.

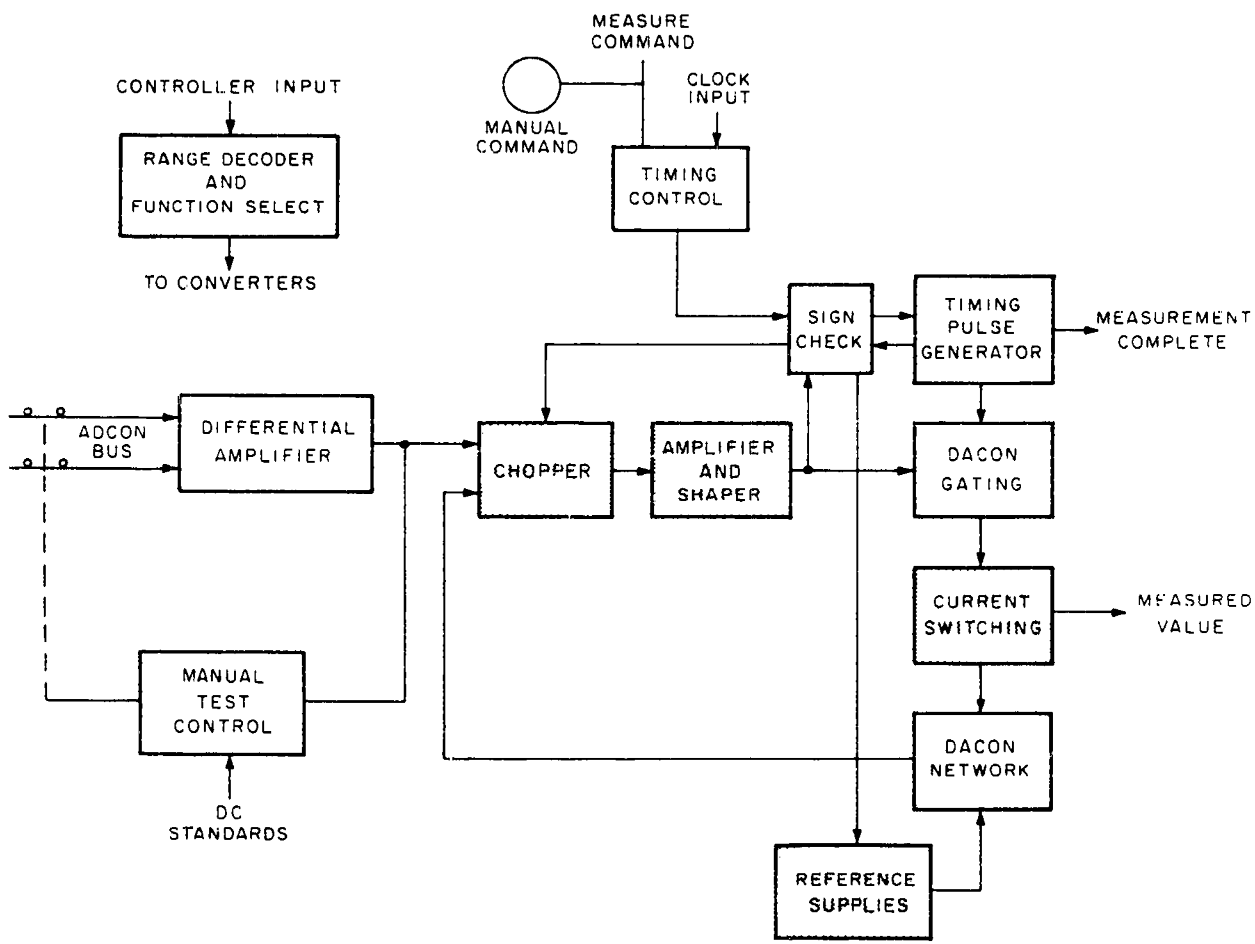


Figure 6-43. Digital multimeter functional block diagram

b. Plans

(1) The Digital Multimeter drafting effort will be completed.

(2) The unit will be released for manufacturing.

J. Data Output Buffer

a. Progress and Status

The design of the Data Output Buffer remains as described in previous reports. All circuit layout has been completed and released to drafting. Chassis wiring diagrams have been started.

b. Plans

During the next quarter this unit will be completed and released for manufacturing.

6.1.7 INTERNAL POWER SUPPLIES

A. Introduction

Progress on Internal Power supplies during the past quarter was concerned with the design, testing, layout and packaging of the unregulated power supplies and of the remote regulators.

B. Unregulated Power Supplies

a. Status and Progress

Drawer sizes for the unregulated power supplies have changed from full-width drawers to half-width, seven-inch drawers (see Figure 6-44). Detail and assembly drawings are complete, and the long-lead items have been released for procurement.

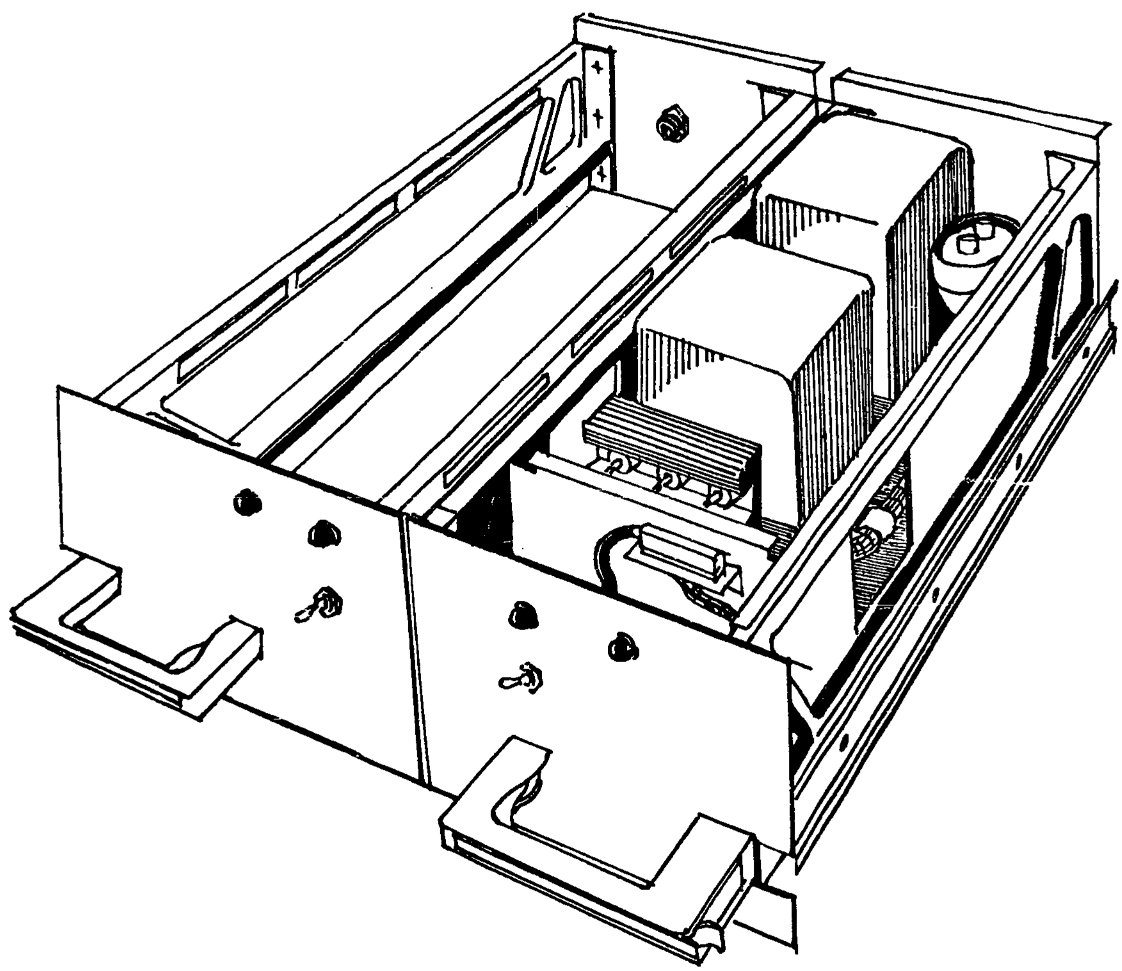


Figure 6-44. Packaging of unregulated dc power supplies

b. Power Supply Design

The schematic for a typical unregulated internal DC power supply is shown in Figure 6-45. All major components have been standardized.

The unregulated output voltages of the DC supplies have been modified to be compatible with the regulator requirements. The current ratings of three of the supplies have been increased as a result of the program for component standardization.

Present versus previous voltage and current ratings of the unregulated DC power supplies are shown in Table 6-3.

Curves showing thermal dissipation in watts versus load in amperes for each of the unregulated supplies are shown in Figure 6-46. These curves show that dissipation is linear from no-load to full-load.

Table 6-3. Previous vs present voltage and current ratings for unregulated power supplies

MTE Number	Nominal dc volts	Voltage (volts)		Current (amps)	
		Previous	Present	Previous	Present
5757	120	120	106	5	5
5754	60	60	56	5	8
5756	30	30	31	5	10
5755	18	16	18	16	20
5753	12	9	12	20	20

C. Regulators

a. General

DC voltage regulation is accomplished by regulator drawers located at the rack where the required voltages are used. There are, at present, nine such regulator drawers in an MTE system. Each regulator drawer contains regulator

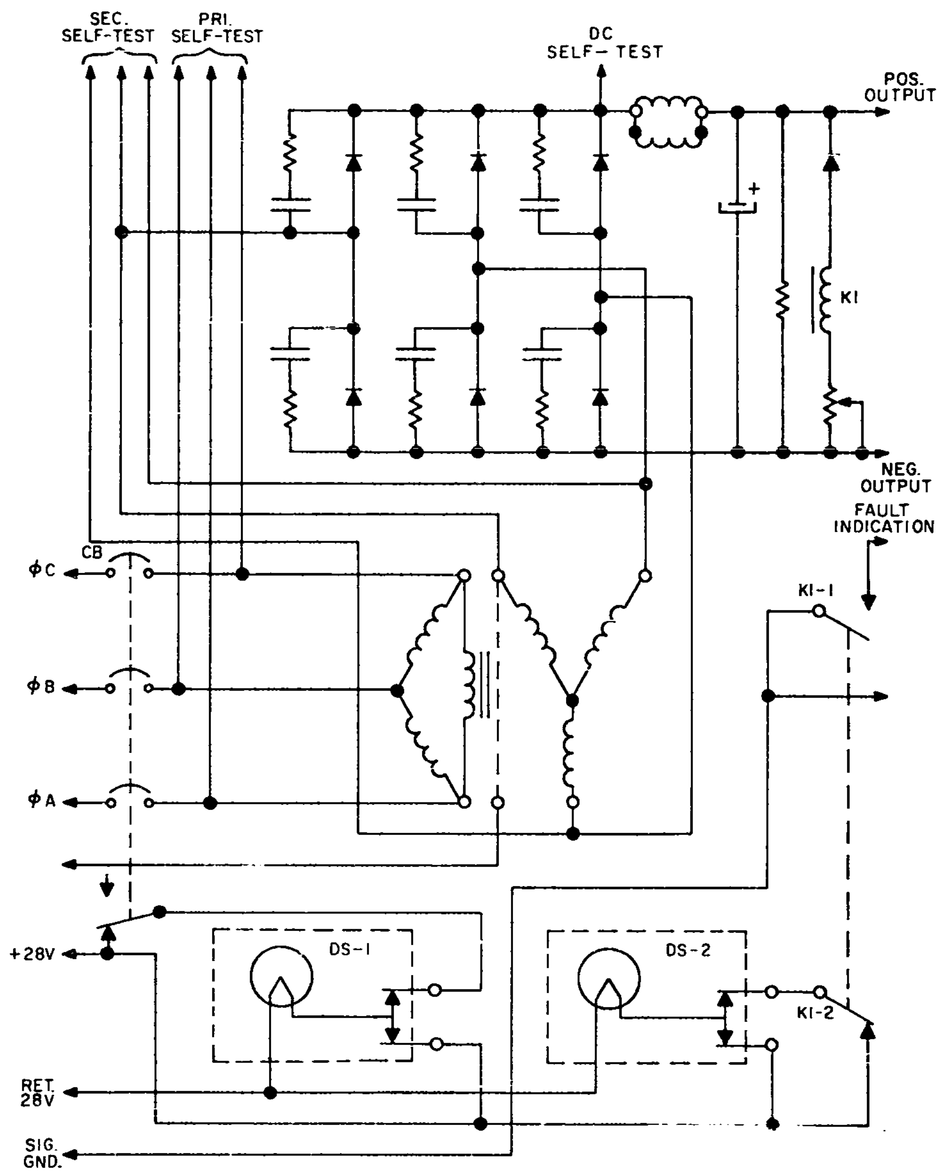


Figure 6-45. Typical interval power supply, schematic

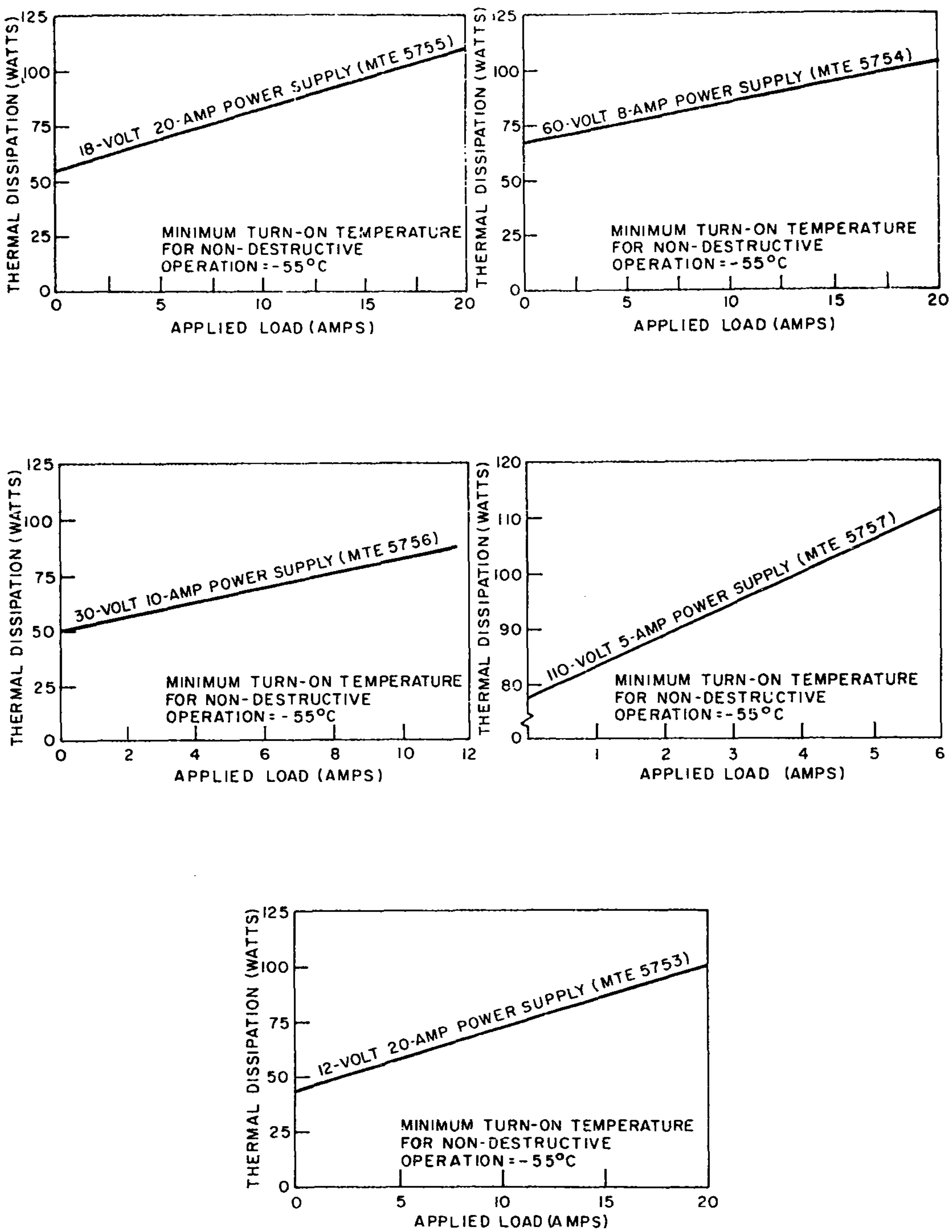


Figure 6-46. Thermal dissipation curves for interval power supplies

cards, pass transistors, and protection devices. Up to thirteen regulator cards and associated pass transistors can be accommodated in each drawer. The outputs from a drawer can be any combination of voltages and multiples of current at each voltage up to the point where the maximum of thirteen cards are used. Each of the nine drawers in the system are different depending upon the voltages and currents required by the portion of the MTE system supplied by each drawer.

Two types of regulator circuits are used; a positive-supply regulator circuit and a negative-supply regulator circuit.

b. Design Current Ratings

The current rating of certain of the regulators were changed during the quarter. Table 6-4 gives the present rating of each regulator and compares these with the previous ratings.

Table 6-4. Capacity of current regulator circuits

Output Voltage	Current Ratings (amps)	
	Previous	Present
+ 3	Not Used	3
- 3	Not Used	3
+ 6	5	5
- 6	5	5
+ 12	4	4
- 12	4	4
+ 25	1.25	3
- 25	1.25	3
+ 50	1.25	2
- 50	1.25	2
+100	1.25	1.25
-100	1.25	1.25

c. Positive-Supply Voltage Regulators

The designs of the positive-voltage regulators have been completed. A schematic diagram of the +12V regulator, typical of the circuits used for the +6V, +12V, and +25V regulators, is shown in Figure 6-47. Relays K1 and K2 provide overvoltage and undervoltage indication. Resistors R22 and R25 allow the standardization of the relays employed in the various regulators.

The remote sensing leads are connected at points A and B of Figure 6-47. Resistors R26 and R27 are employed in the voltage divider string (R15, R16, and R17) to ensure that the circuit will remain regulated even if one of the remote sensing lines is broken. If remote sensing is not needed, R26 and R27 are shorted out.

A schematic diagram of the +50V regulator circuit, used also for the +100V regulator, is shown in Figure 6-48. In order to allow the same zener diode to be used in all regulator circuits, it was necessary to modify the configuration of the regulator circuit at the higher voltages. Relay R1 provides undervoltage indication; no overvoltage indication is required in the +50 and +100V regulators. The remote sensing leads are again connected at points A and B.

A set of calculations of loop gain, output resistance, AC stability, and breakpoints, including a Bode stability diagram is contained in Appendix H. Although specifically for the +12 volt regulator, these calculations are representative of the design procedure followed for all the positive regulator circuits.

One universal breadboard was constructed and successively modified as necessary to test each of the positive-supply voltage regulators for load regulation, line regulation, and output ripple. All the regulators met or exceeded specifications, and no signs of oscillation were found (see Table 6-5). Since the +6V regulator has the highest dissipation of any of the circuits, this circuit was subjected to temperatures over the range -18°C to +52°C while both load and line regulation were checked, results were satisfactory.

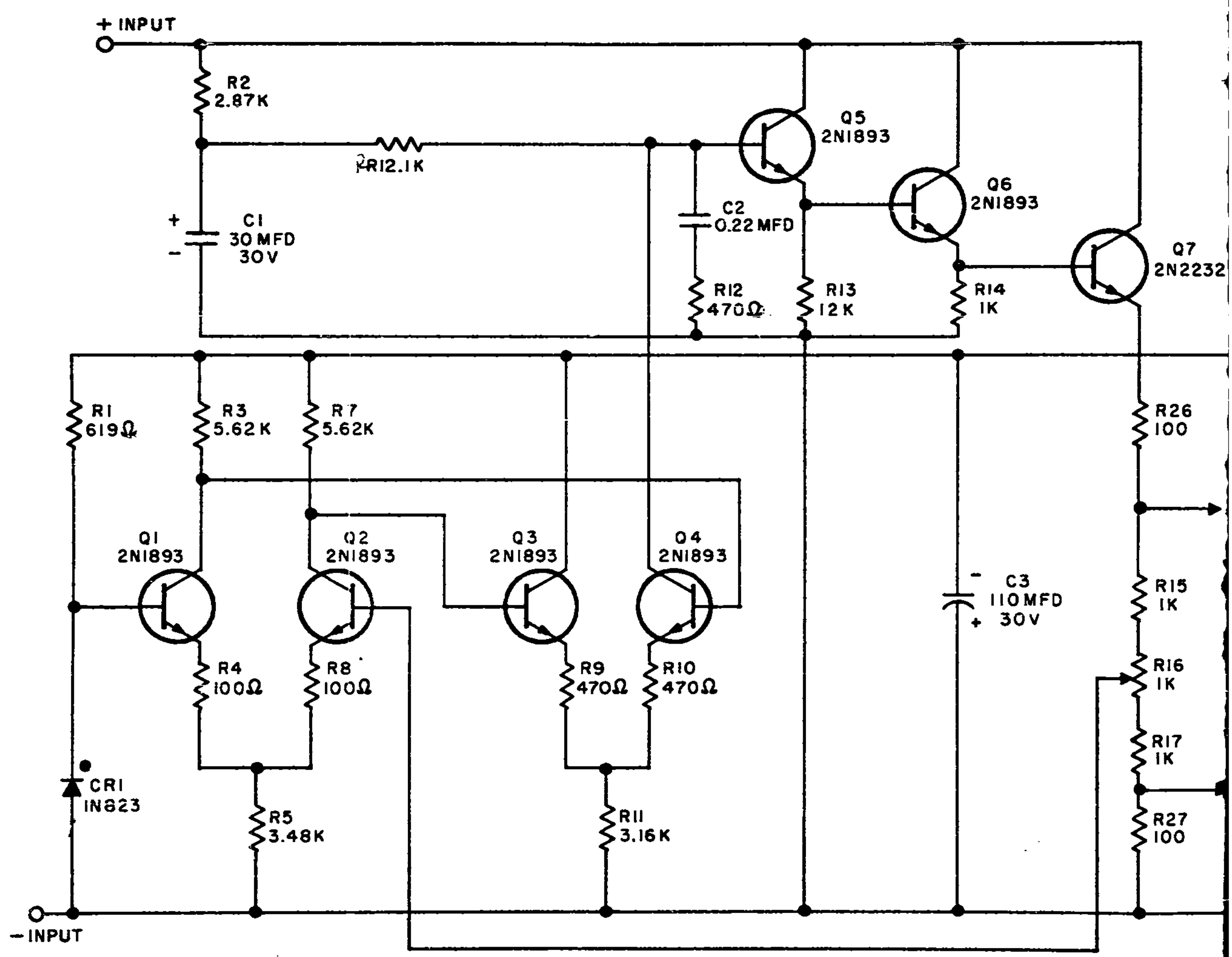


Figure 6-47. +12 vdc regulator circuit

1

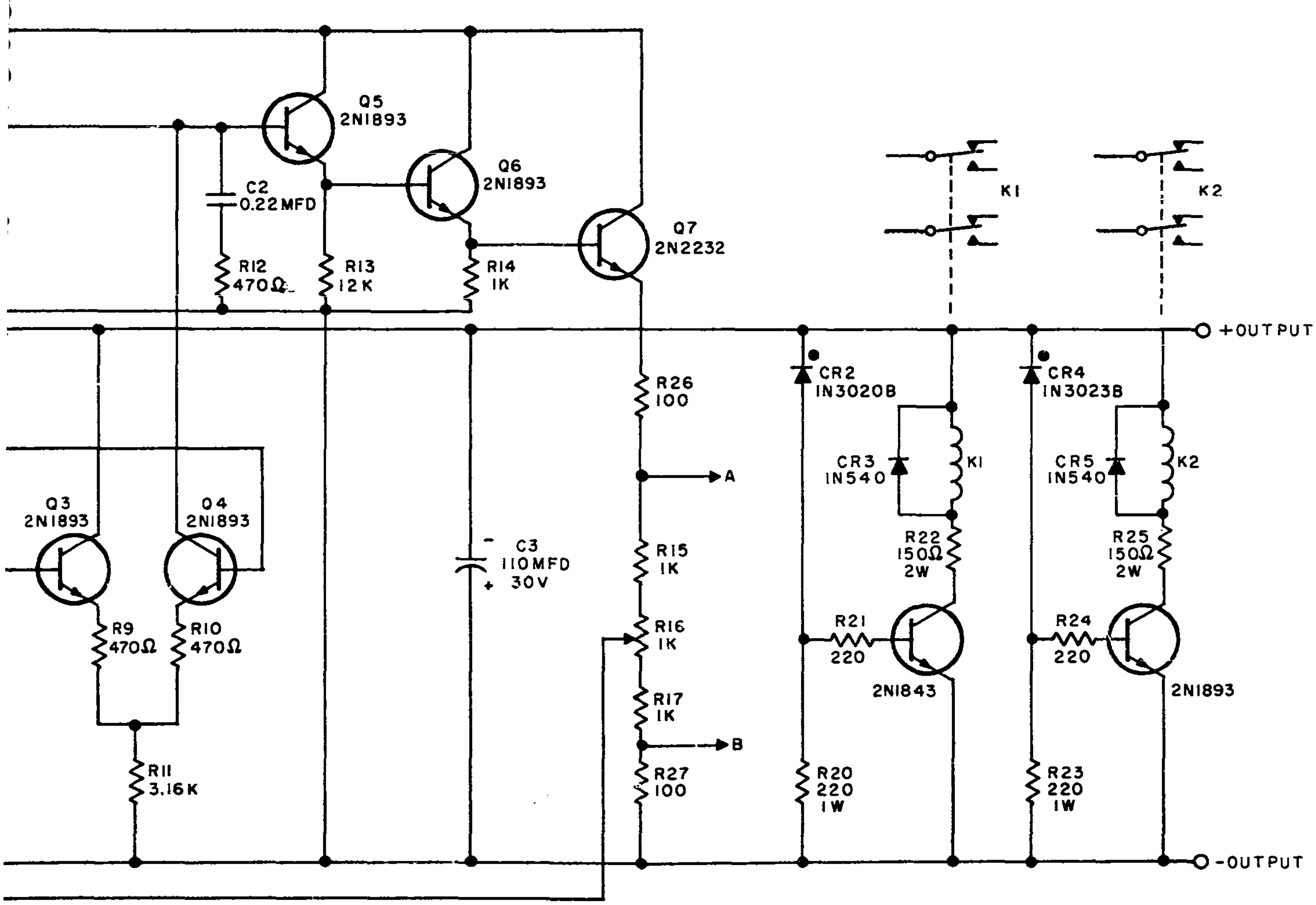


Figure 6-47. +12 vdc regulator circuit

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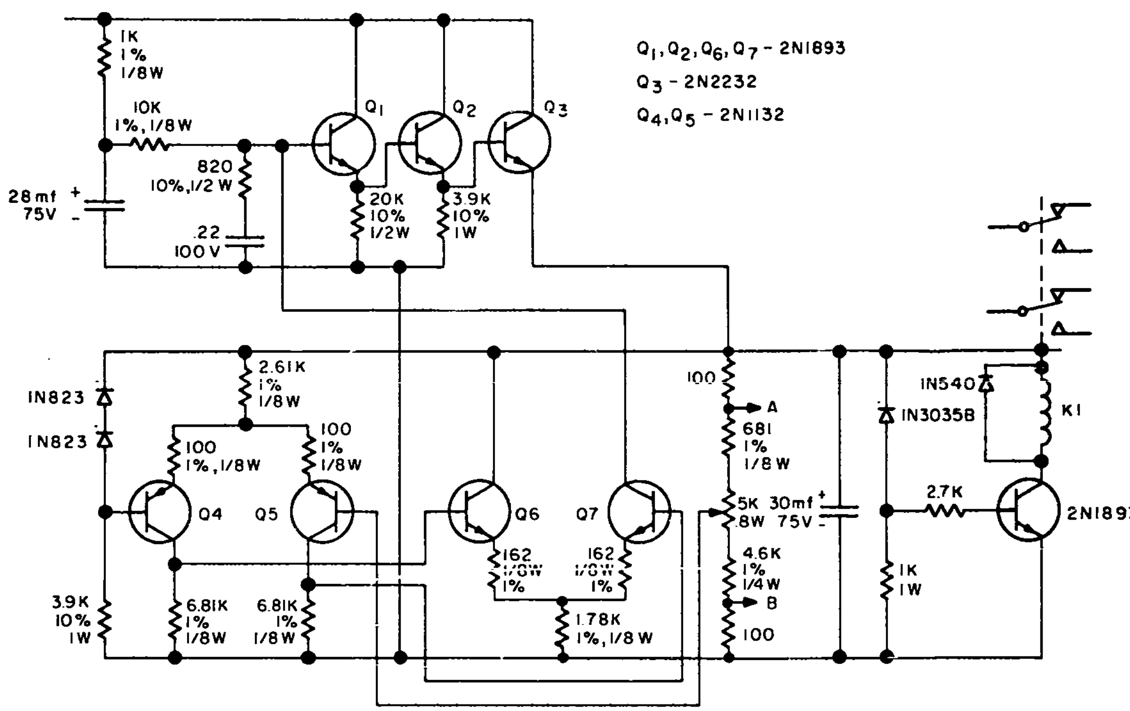

Figure 6-48. +50 vdc regulator circuit

Table 6-5. Positive-supply voltage regulator, test result

Regulator	Load Regulation*	Line Regulation**	Ripple (Max)
+ 25V	0.004V	0.014V	0.4 mV
+ 12V	0.006V	0.022V	0.5 mV
+ 50V	0.010V	0.020V	1.0 mV
+100V	0.100V	0.150V	1.0 mV
+ 6V	0.008V (+25°C)	0.016V (+25°C)	0.5 mV (+25°C)
	0.006V (-18°C)	0.016V (-18°C)	0.5 mV (-18°C)
	0.010V (+52°C)	0.016V (+52°C)	0.5 mV (+52°C)

* Full-Load to No-Load

** For ± 5% Line Voltage variation to unregulated supply

Printed circuit board layout of the positive regulators has been started. Each regulator will fit on one standard MTE planar board. The only long-lead items in these regulator circuits are the relays; these have been released for procurement.

d. Negative-Supply Voltage Regulators

The negative-voltage regulator circuits differ from those used in the positive regulators in order to prevent the paralleling of loads and to allow the same type pass transistor to be used in both circuits. The design used for the negative regulator circuits is shown in Figure 6-49. The negative 12V and 50V regulators have been breadboarded and preliminary line and load regulation tests have proved satisfactory.

Design and breadboard tests of all negative-supply voltage regulators will be completed during the coming quarter.

e. Heat Dissipation

Curves of thermal dissipation in watts versus applied load in amperes are shown in Figure 6-50. The dissipation curve for a positive regulator is the same as

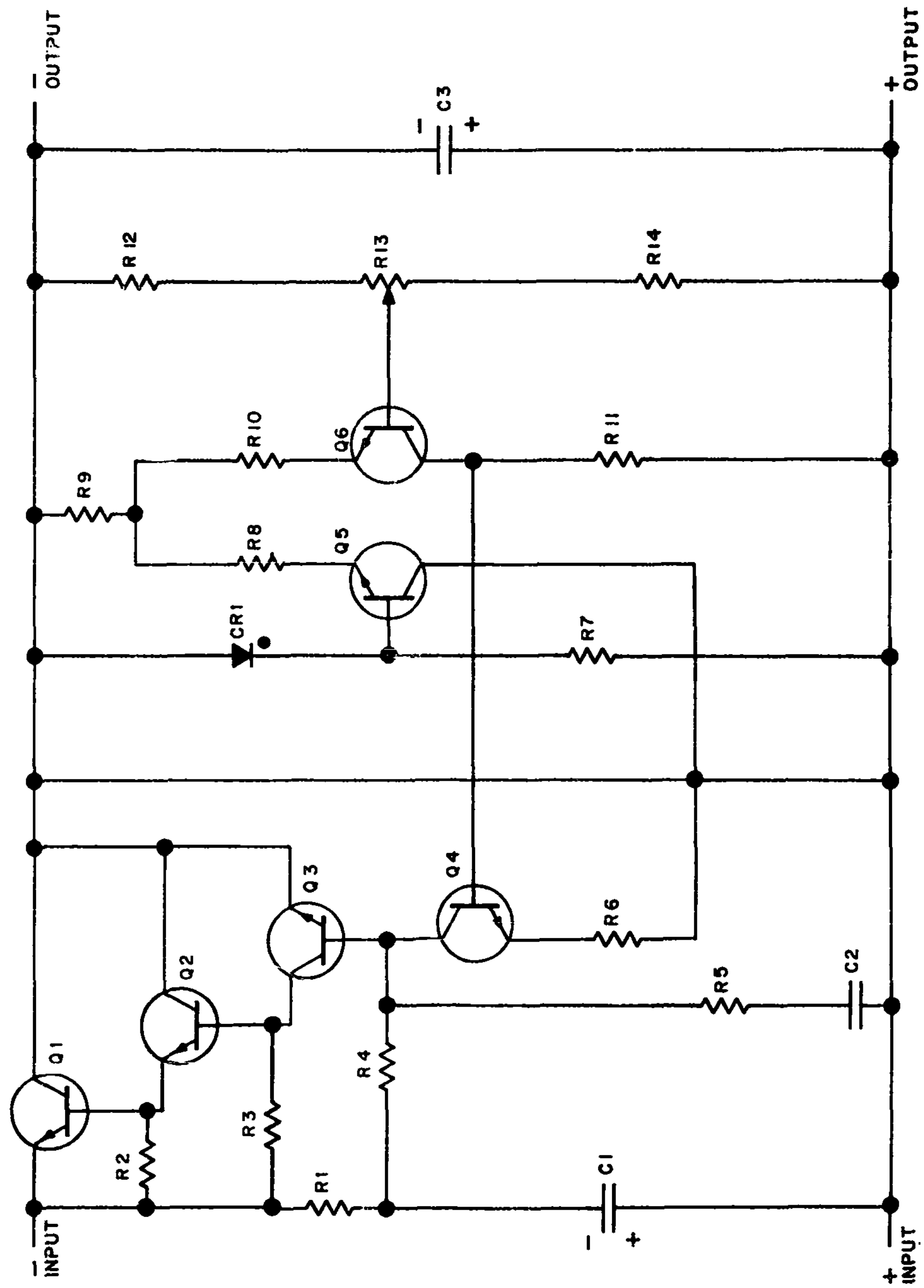

Figure 6-49. Negative - supply voltage regulator schematic

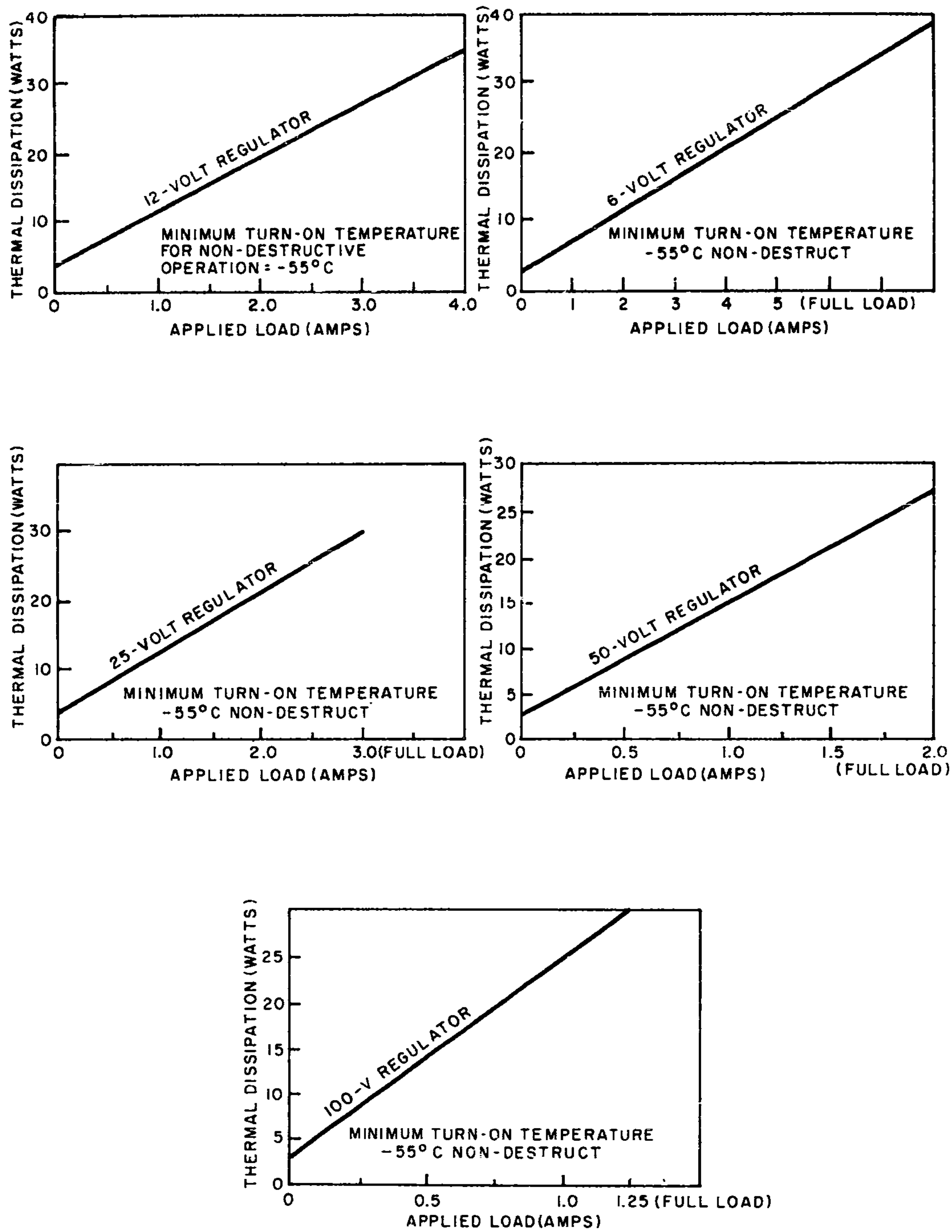

Figure 6-50. Thermal dissipation curves for voltage regulators

for a negative regulator of the same voltage. These curves show the dissipation to be linear between no-load and full-load.

A fin-type heat sink has been selected for use with the pass transistors. Figure 6-51 shows the calculations used in determining the performance of this heat sink.

f. Plans for Next Quarter

Work on regulators for the coming quarter will include:

(1) Completion of design of the negative-supply voltage regulators.
(2) Completion of mechanical layout for the regulator drawers.
(3) Completion of the regulator drawing package consisting of assembly drawings, printed circuit card layouts, card and silk screen details.

6.2 HYDRAULIC TEST SET

6.2.1 INTRODUCTION

This section reports equipment development progress for those items that are peculiar to or associated only with the Hydraulic Test Set.

6.2.2 HYDRAULIC AND PNEUMATIC TEST STANDS

A. Test Stand Subcontract

On 24 January 1963, Greer Hydraulics Inc., Los Angeles, California was awarded a subcontract to perform studies, make investigations, design, develop, fabricate and test a Hydraulic Test Stand and a Pneumatic Test Stand.

The Stands must initially be capable of testing the hydraulic and pneumatic sub-systems of the Mauler Missile System and must possess the capability of testing similar equipment sub-systems of the nine other missile systems specified. The stands are to be designed with sufficient flexibility to permit extension to the testing of hydraulic and pneumatic sub-systems of future missile systems.

Silicon Power Transistor - 2N2232

Maximum allowable junction temperature = 150°C

Thermal resistance = 0.5°C/watt, case to junction

Maximum power dissipation - 36.5 watts

Mica Insulator

Thermal conductivity = $0.009 \frac{\text{watts}}{\text{in. °C}}$

Thickness = 0.003 in. max

Area = 0.331 in.^{2}

Heat Sink

Wakefield Engineering Co. No. 403

Thermal Resistance = 1.85°C/watt,
for vertical mount and natural convection

Cooling Air

Natural convection

Average air temperature = 25.5°C

Calculation of Maximum Transistor - Junction Temperature

Heat-sink rise = (1.85°C/watt)(36.5 watt) = 67.5°C

$$\text{Heat-sink-to-case rise} = \frac{(36.5\text{ watt})\,(0.003\text{ in.})}{(0.009\text{ watt }^{\circ}\text{C in.})\,(0.331\text{ in.}^2)} = 36.5^{\circ}\text{C}$$

Case-to-junction rise = (0.5°C/watt) (36.5 watt) = 18.2°C

Maximum junction temperature = 25.5 + Σ rises = 147.7°C

Figure 6-51. Heat-Sink Calculations for Voltage Regulators

(1) Open-loop flow-gain measurements - This involves a very accurate application of the maximum differential current (both positive and negative) to the servovalve and measurements made on the valve-flow characteristics.

(2) Valve unbalance - This is accomplished by holding the valve in a closed-loop quiescent condition and measuring the differential current necessary to overcome any hydraulic or mechanical unbalance present in the valve.

(3) Internal leakage - This is accomplished by holding the valve in a closed-loop quiescent condition and measuring the exhaust leakage from the valve.

These techniques, plus the hardware implementation necessary to accomplish these types of servovalve testing, serve a two-fold objective. The first is to qualify all servovalves in an automatic mode; the second is to provide capability to set up a rebuilt valve in accordance with proper specifications.

One additional type of test that should be included, primarily to determine valve rejects caused by hysteresis[1], is a frequency response test. If a frequency response technique of valve testing were not employed, this hysteresis information would have to be derived by a manual method.

The frequency response test requires that the valve be driven sinusoidually (while in a closed-loop condition) and a phase lag measurement made between the input signal and the output flow. The set-up is identical with that used in the valve unbalance test, except that additional equipment is necessary to supply sinusoidal input to drive the valve through the DC amplifier. The Time Interval and Frequency Meter (MTE 5777) is used to make the phase lag measurements, converting frequency to time difference. Schematically, this requires a set-up as shown in Figure 6-58.

1. Hysteresis in a servovalve is defined as the amount of differential current necessary to overcome dead space, friction, and torque motor or solenoid residual magnetism.

B. Specific Objectives

The subcontract scope of work has been broken down into the following specific tasks:

Task I. Technical Requirements Analysis

The objective of this task is to gather information on the components of the various missile hydraulic and pneumatic systems to establish system parameters for the Hydraulic and Pneumatic Test Stands. While accomplishing this, the hydraulic and pneumatic systems state of the art will be determined and will be projected to parameters envisioned for the 1967 era. This data will then be compared to contemporary state of the art parameters as exemplified by current Mauler system requirements and the system requirements of the nine other missiles. This task is scheduled to be completed by 15 May 1963, when a task report is to be submitted to RCA. In actuality, this task will continue throughout the course of the program in that information gathering and comparisons between current and anticipated parameters will be conducted until the unit is delivered.

Task II. Physical Parameters Study

The objective of this task is to establish the physical parameters of the units from the information gathered in Task I and from specifications and instructions received from RCA.

Task III. Design and Developments

The objective of Task III is to formulate a design for the Hydraulic and Pneumatic Test Stands which will meet the requirements of the RCA purchase description and which will contain the capabilities determined necessary from the above study tasks and from the RCA specification.

Task IV. Fabrication of the Development Model

The objective of Task IV is to fabricate one Hydraulic and one Pneumatic Test Stand to conform to the design and development projected in Task III and to deliver the Test Stands to RCA at the prescribed time.

Task V. Test Procedures and Programs

The objective of Task V is the establishment of test procedures and test programs for components of the various missile systems under examination and to define test procedures and programs for the Hydraulic and Pneumatic Test Stands. During this task, the requirements of the various missile components to be tested will be coordinated with the equipment design and development phase to insure the capability of the end items to meet or exceed all requirements of the purchase description and subsequent addenda thereto.

Task VI. Documentation

The objective of this task is to establish and maintain comprehensive documentation which will reflect the progress, effort and accomplishment embodied in each and every task in the purchase description. When complete, it will encompass engineering drawings which will enable reproduction of the unit, manuals describing actual operation and maintenance, description and theory of design, schematics and test procedures for the unit. Monthly, quarterly and final reports are a responsibility under this task. Production and scheduling reports which trace the development of the unit from purchase order to delivery are a requirement.

Task VII. Product Assurance

The objective of Task VII is to establish a product assurance program which will be based upon requirements for a high degree of reliability and safety, combined with value engineering and maintainability to attain end items that will possess the highest reliability and maintainability factors which are commensurate with current and projected missile systems and their requirements.

Task VIII. Special Tools and Test Equipment

The objective of Task VIII is to provide with the end items, all special tools and special test equipment that will be needed during acceptance testing, calibration, and maintenance of the test stands.

Task IX. Leads and Connectors

The objective of Task IX is to provide all leads, connectors and adaptors necessary to connect the component (UUT) of any missile system covered by the RCA purchase description to the test stands.

C. Progress

a. General

The initial efforts of the subcontractor, during February, consisted of an indoctrination by RCA of responsible Greer personnel. The following areas were covered: (1) detailed Mauler data, (2) general hydraulic/pneumatic data on other missile systems, and (3) detailed MTE systems data with emphasis on the HTG Controller-Stimulus Measurement areas. Therefore the larger portion of the following progress reflects the efforts of the month of March. In addition, although Tasks I and II include efforts toward both the Hydraulic and Pneumatic objectives, design of the pneumatic test stand (Task III) must await AMICOM approval.

Through the month of March, Greer continued the Technical Requirements Analysis Study and the Physical Parameters Study to gether Hydraulic and Pneumatic Test requirements information on the ten missile systems. Preliminary systems schematics have been drawn and preliminary systems functions have been determined.

From 11 March through 14 March 1963, the initial Status Review Meeting was held with RCA at the Greer facility. On 28 and 29 March 1963, a Preliminary Product Assurance Design Review was held by RCA at the Greer facility.

A program organizational chart, responsibility charts, milestone charts*, reporting schedule and manpower assignment charts were finalized in anticipation of phasing in Task III, V, VI, and VII during the month of April.

b. Task I - Technical Requirements Analysis

1. General

Component investigation efforts have been concentrated on the Mauler Missile System. A total of 89 hydraulic components on both the azimuth system and the rotating platform were investigated. This is the total quantity of hydraulic components in the Mauler launcher pod.

Of the 25 components in the azimuth drive system, a total of 20 components have been identified by vendor part number. However, 8 of these parts are manifolded in with major components and require further investigation. The 5 remaining components have been identified by Food Machinery and Chemical Corporation (FMC) part number. Individual drawings and component specifications for a total of 13 components in this system have been obtained.

On the rotating platform, the hydraulic systems contain 64 components. Twenty-six of these components have been identified by vendor part number, 19 by FMC part number. The components that have not been identified in this system are in the Raytheon-manufactured radar systems.

In conjunction with the component study, the Mauler overall requirements are being used as a guide in the physical parameters study.

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* Some of the Major Milestones are:

15 May 1963	Study Completion (by Greer)
30 May 1963	Concept Approval (by RCA)
1-15 June 1963	Long Lead Release (by Greer)
30 June 1963	Data Updating (by Greer)
15 Dec 1963	Hydraulic Test Stand Delivery (at RCA)
30 Dec 1963	Pneumatic Test Stand Delivery (at RCA)

2. Technical Data Received by Greer

Mauler:

Checkout and Operating Instructions Pod 2 dated 5/15/62

Checkout and Operating Instructions Pods 3 and 4 dated 10/17/62

Addendum to above dated 2/1/63

Synopsis on Mauler from RCA Library Data

FMC Drawings:

1075967	Solenoid Valve	Rotating Platform
1076006	Manifold Assembly	
1076647	Manifold Assembly	
1076648	Manifold Assembly	
1076807	Manifold Assembly	
1075611	Manifold Block	Azimuth Drive
1075612	Manifold Block	

TM 246-351 Mauler Aft

19 additional drawings from component manufacturers

Other Missiles:

Hawk:

Synopsis from RCA Library

Pershing:

Drawings on Ground Support Pneumatics System

Pertinent Data from Martin Co., Notes on Development Type Matl., Vol 1410-1, September 1961

Sergeant:

Dwg. #PD10062588 Launcher Hydraulic System

Nike Hercules:

Document on Hydraulic Pumping Unit

Lacrosse:

Hydraulic System Schematic and Discription

3. Manufacturers Contacted by Greer

Vickers, Inc., on pumps and motors used on Mauler

Denison Engineering Co., on latest version of 500 Series Pump

Permanent Filter, on components used on various Army missile systems

Aircraft Porous Media, same as above

Cornelius Compressor Co., on Pneumatic Power Supply for Pershing

York Air Brake Co., on rotating hydraulic components for Hawk

General Electric, on 400 cycle main pump drive motor

Louis Allis Co., same as above

4. Fault Isolation

From the Technical Requirements Analysis Study accomplished to date, it has been concluded that the Mauler missile possesses the capability to isolate faults in its hydraulic system down to the components level and/or replaceable subsystems. In most cases this capability depends on the skill and familiarity of the operator.

5. Electrical System

The program commands and stimuli supplied by the controller-stimuli-measurement equipment to the Hydraulic Test Stand were studied. These BCD inputs define, in part, the servo loops and input control devices in the Hydraulic Test Stand. Studies were also made of the required outputs from these servo loops and control devices. Toward this end, studies were made in the following areas.

(i) Methods of starting the motors were investigated. Large power consumption in small packages necessitates the use of aircraft type equipment. Y-delta starting will be used to further reduce the inrush current from the generator.

(ii) Another study is being conducted to establish the overall parameters for voltage, current and frequency stimuli. Particular attention was given to worst direction tolerances for voltage and current. Regulation, frequency and ripple are presently being considered for the various electrical systems in the Hydraulic Test Stand.

(iii) Methods of indicating malfunctions in the Hydraulic Test Stand were studied. A differential amplifier is being designed to monitor output versus input and when a differential tolerance is exceeded, a signal will send a malfunction indication to the Controller.

c. Task II - Physical Parameters Study

1. General

The following information indicates the initial effort in defining the hydraulic test stand system based on Mauler and other missile system requirements. These accomplishments are tentative approaches based mainly on the RCA Purchase Description and shall in later months be influenced by the Hydraulic/Pneumatic TRA effort.

The approach being taken in the physical parameters study is to reduce component size and weight to a minimum. The possibility exists that enough space will be available within the Hydraulic Test Stand to incorporate a small ultrasonic cleaning unit as well as capability for sampling fluid contamination and viscosity. No problems are expected in meeting the space and technical requirements of the TRA. The strict approach to miniaturization is to obtain sufficient space within the envelope specified to provide as many additional features as possible.

2. Module Design

The intention, as outlined in Greer's original proposal, is to design the equipment as four separate modules. The preliminary functional block diagram (Figure 6-52) indicates the modularization for the various functions within the Hydraulic Test Stand. Each module is planned to be removable for maintenance.

(i) Power Supply (see Figure 6-53)
Hydraulic fluid is drawn from the reservoir by fixed volume pump (3), excess flow from this pump not utilized by the main

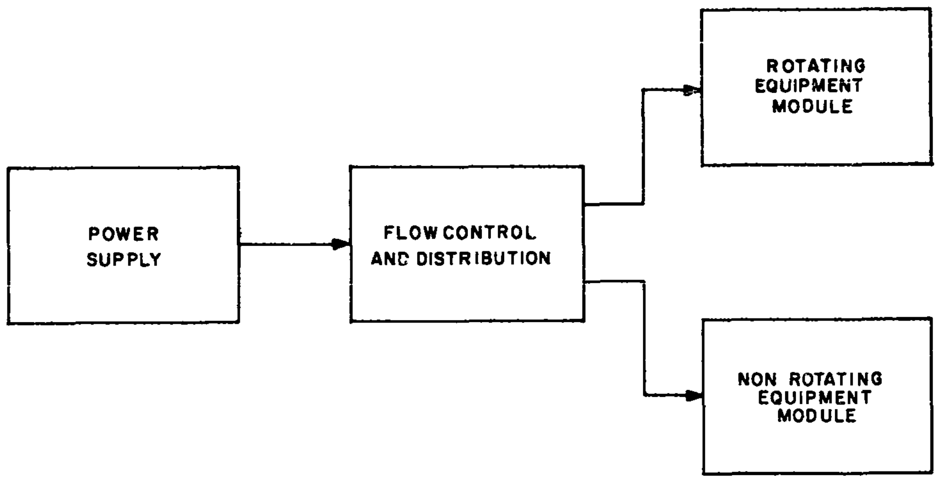


Figure 6-52. Hydraulic Test Stand - functional block diagram

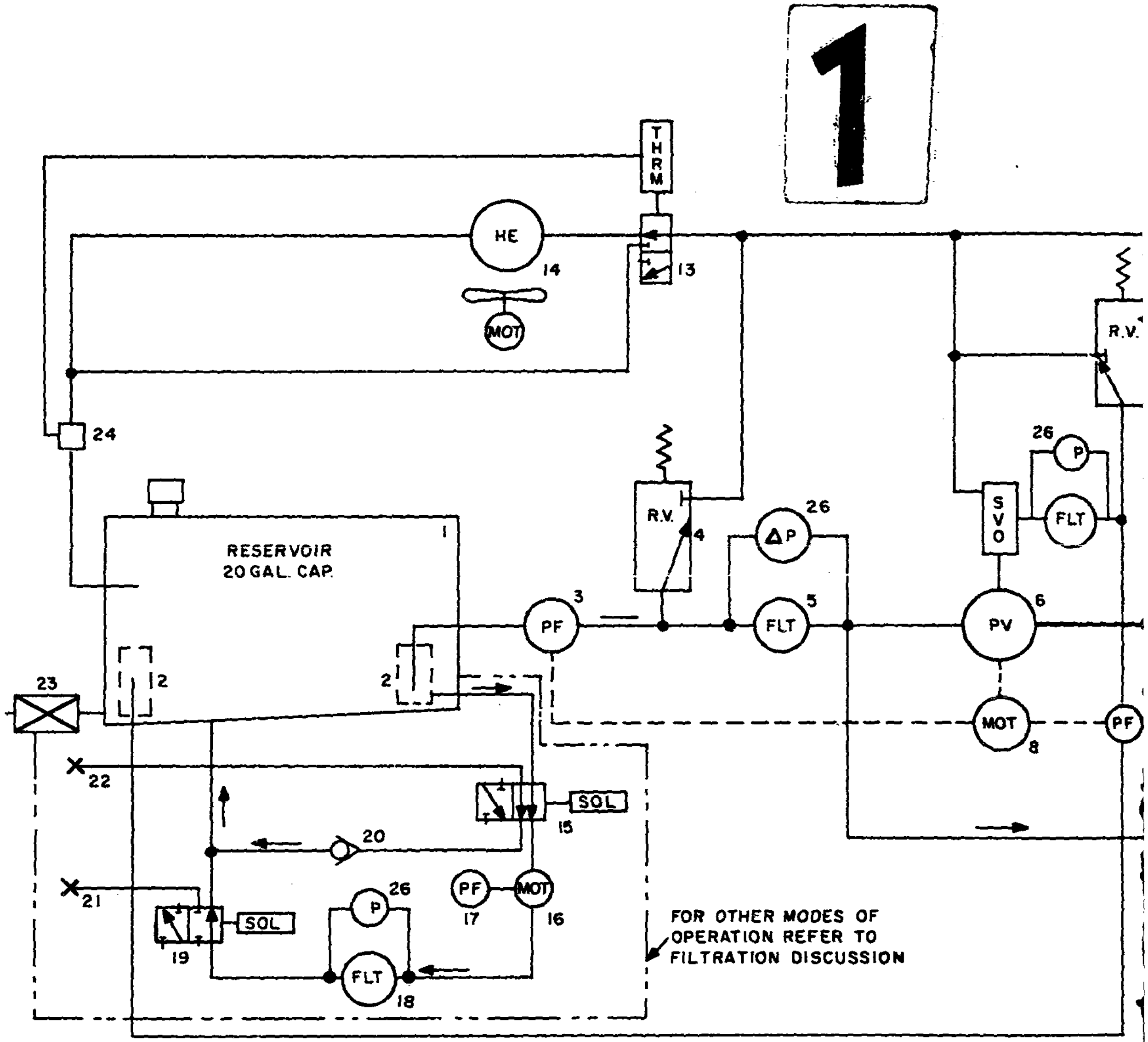
pump (6) is bypassed to the return line through relief valve (4). The chief purpose of pump (3) is to prevent cavitation in the main pump (6).

The output from the main pump (6) is adjusted by an integral servo control to limit the output in accordance with the required flow, thus conserving power and limiting generation of heat. The servo is hydraulically operated by a separate source of hydraulic power supplied by pump (7). Excess fluid not required by the servo control is bypassed to the return line through relief valve (10). The three individual pumps (3), (6) and (7) are integral parts of a single pump driven by a single motor.

Output of the main pump is limited to its maximum safe output pressure by pilot operated relief valve (11). This relief valve also serves as a dump valve for emergency shutdowns. When required to shut down instantaneously, solenoid valve (12) would be de-energized (fail safe) by shutting off its operating voltage. All output pressure would then be relieved to the return line.

Fluid is returned through modulating thermal valve (13). This valve returns all fluid directly to the reservoir until warmup is complete. At the higher operating temperatures, fluid flow to the reservoir is through heat exchanger (14).

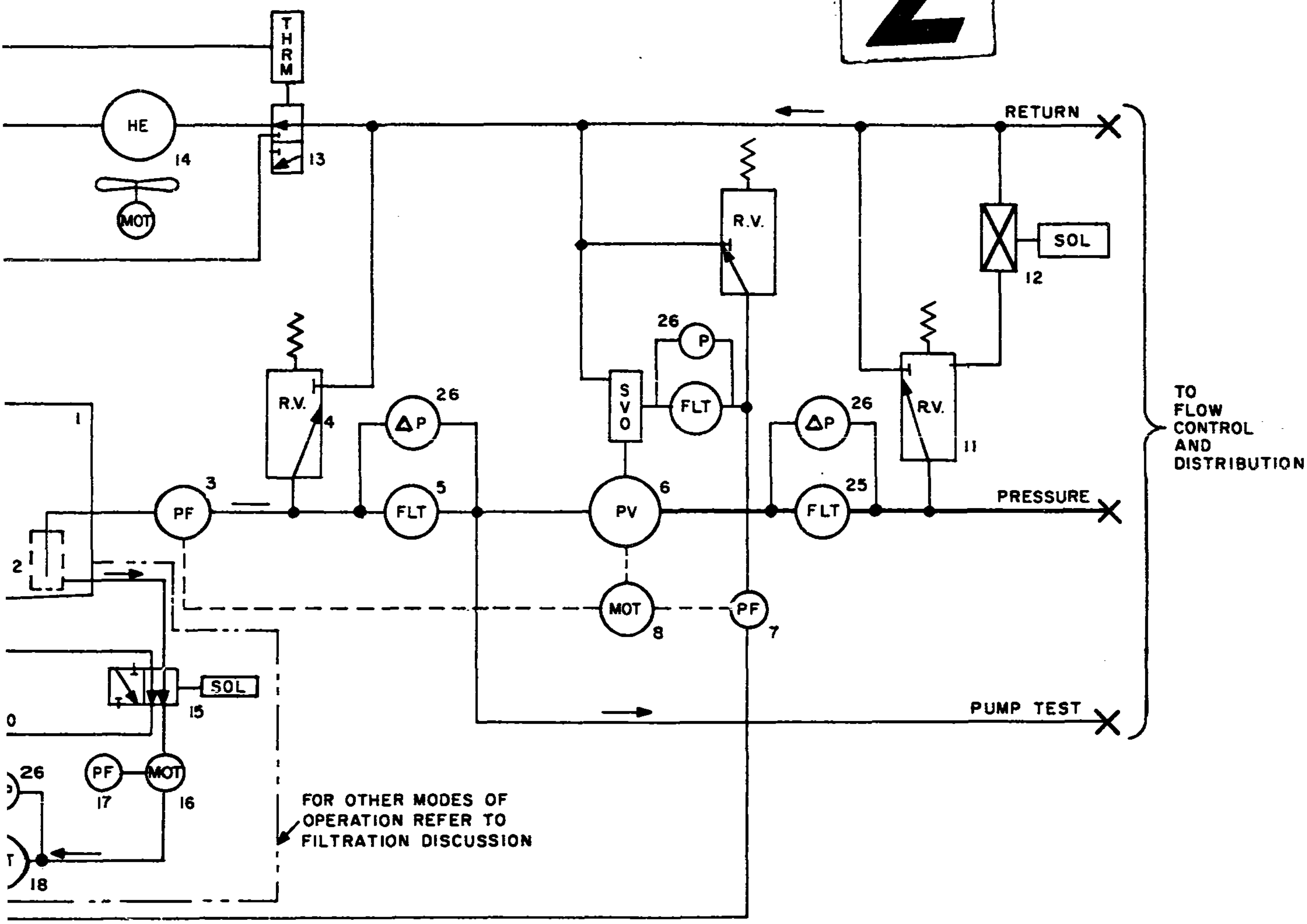
The physical parameters on the power supply module will be finalized as soon as information is received from the manufacturers on the 400-cycle motors. Adequate information is available on all other vendor components to be used in this module o complete a design study.



ITEM NO.	NO. REQD	NOMENCLATURE	ITEM NO.	NO. REQD	NOMENCLATURE
1	1	RESERVOIR 20 GAL CAP. ALUM	10	1	RELIEF VALVE
2	2	STRAINER - SUBMERG TYPE	11	1	RELIEF VALVE
3	1	PUMP - FIXED DISPLACEMENT	12	1	VALVE - SOLENOID
4	1	RELIEF VALVE	13	1	THERMAL MIXING VALVE
5	1	FILTER	14		HEAT EXCHANGER UNIT
6	1	PUMP - VARIABLE DISPLACEMENT	15	1	VALVE 2 POSITION - 3 WAY - SOLENOID
7	1	PUMP - SERVO	16	1	PUMP-FIXED DISPLACEMENT
8	1	MOTOR - ELECTRIC	17	1	MOTOR - ELECTRIC INTEGRAL WITH 16
9	1	FILTER	18	1	FILTER - LOW PRESS. 10 MICROW

Figure 6-53. Power supply - schematic diagr

2



LATURE	ITEM NO.	NO. REQD	NOMENCLATURE	ITEM NO.	NO. REQD	NOMENCLATURE
ALUM	10	1	RELIEF VALVE	19	1	VALVE-SOLENOID 2 POSITION-3 WAY
E	11	1	RELIEF VALVE	20	1	CHECK VALVE
IENT	12	1	VALVE-SOLENOID	21	1	PORT
	13	1	THERMAL MIXING VALVE	22	1	PORT
	14		HEAT EXCHANGER UNIT	23	1	VALVE-RESERVOIR DRAIN
CEMENT	15	1	VALVE 2 POSITION-3 WAY-SOLENOID	24	1	SENSOR-THERMAL MIXING VALVE
	16	1	PUMP-FIXED DISPLACEMENT	25	1	FILTER
	17	1	MOTOR-ELECTRIC INTEGRAL WITH 16	26		DIFFERENTIAL PRESSURE INDICATOR
	18	1	FILTER-LOW PRESS. 10 MICROW			

Figure 6-53. Power supply - schematic diagram

It is currently planned to operate the hydraulic pump at the highest practicable speed in order to reduce weight and size; a speed of 4000 rpm is being considered. This, however, will introduce some noise level problems. Denison is running noise level tests on their pump for this use. When the test results have been obtained, a decision will be made as to whether or not acoustic insulation will be required in the hydraulic power supply module.

Because of the low efficiencies obtainable from 400-cycle electric motors, it will be necessary to ventilate these motors from the outside of the shelter. A separate duct will be provided to conduct air to the 400-cycle motors directly from the exterior of the shelter and to exhaust this air from the shelter again.

(ii) Flow Control and Distribution (Figure 6-54)

This unit provides servo controlled flow (or pressure) for the various tests. The servo control also incorporates a variable relief valve to protect the UUT against pressure surges. For each set test pressure, the relief valve is set at a fixed percentage above the programmed value and protects the component against over pressurization.

Flow is directed to the desired test module by the use of solenoid directional valves. Fluid pressure, temperature, and flow monitoring are provided.

Discussions have been held with several flow transducer manufacturers but until further component data is received, it is not possible to finalize these items. This, of course, delays progress on the fluid control and distribution module; however, no impediment is foreseen to completing the physical parameter study of this module within the required schedule.

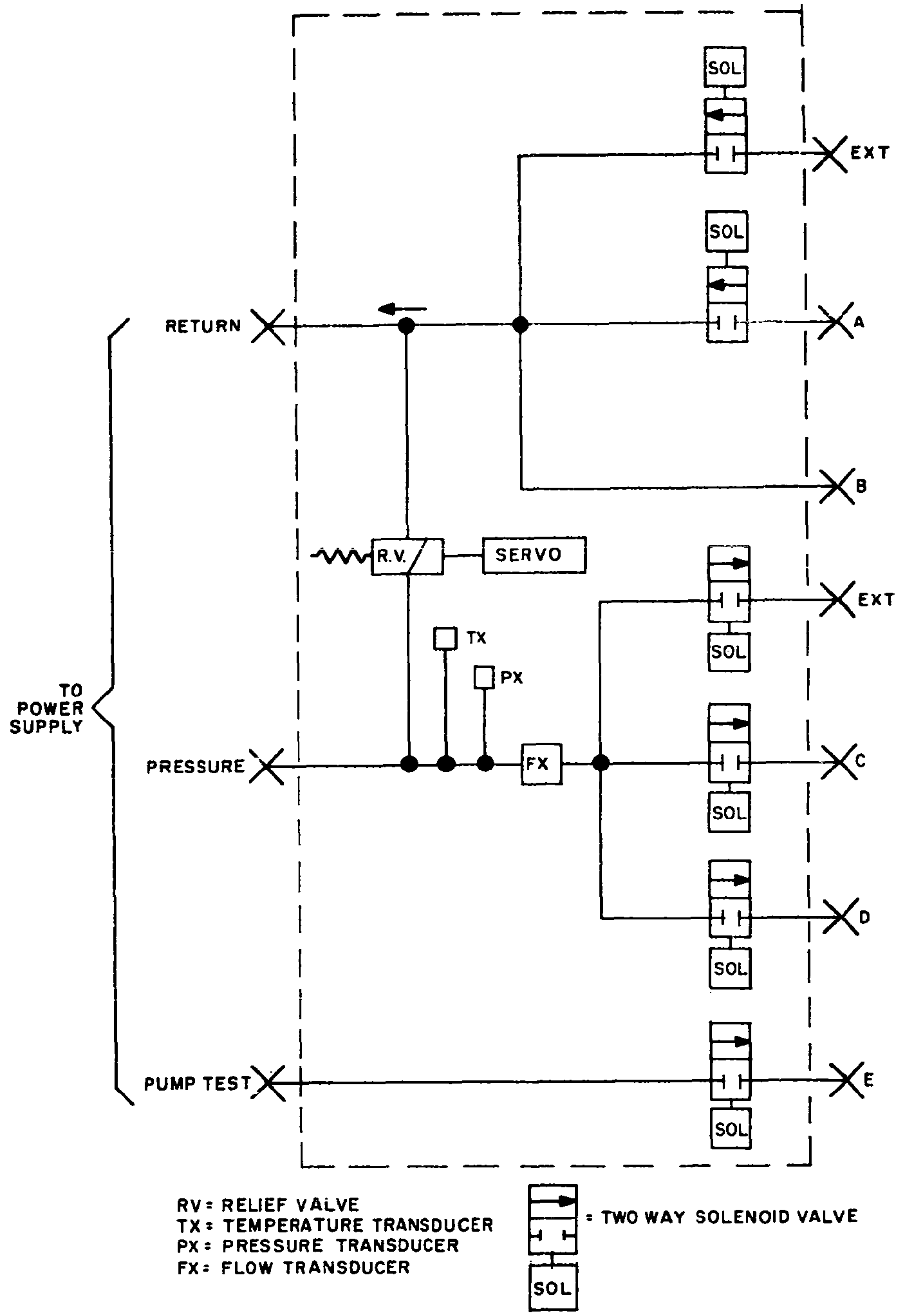


Figure 6-54. Flow control and distribution - schematic diagram

(iii) Nonrotating Equipment Test Module (Figure 6-55)

A nonreversing flow is provided at connection M; the return connection is provided at H. A UUT connected across these terminals is supplied with the desired hydraulic pressures.

If a proof pressure test is to be made, solenoid valves apply hydraulic pressure to the intensifier which provides the desired static pressure to the UUT; the solenoid valve at H is closed in this instance.

Reversing flows for gimbal systems or actuators are available at K and L.

Leakage measurement capabilities are provided by using port G for the return connection.

The selection and design of transducer fixtures, etc., for this module will have to wait until more complete component data is available. Preliminary design studies were started, however, based on the overall requirements.

If possible, this module will run lengthwise at the front of the sink. Connections to UUTs will be made directly from the module.

(iv) Rotating Equipment Test Module (Figure 6-56)

Rotational force is supplied by the hydraulic motor and is applied through the drive pod to devices such as hydraulic pumps, electric generators, and tachometers. The drive pod incorporates torque application and clutching arrangements. If the UUT is an electrical or hydraulic motor, loading may be provided by the torque device.

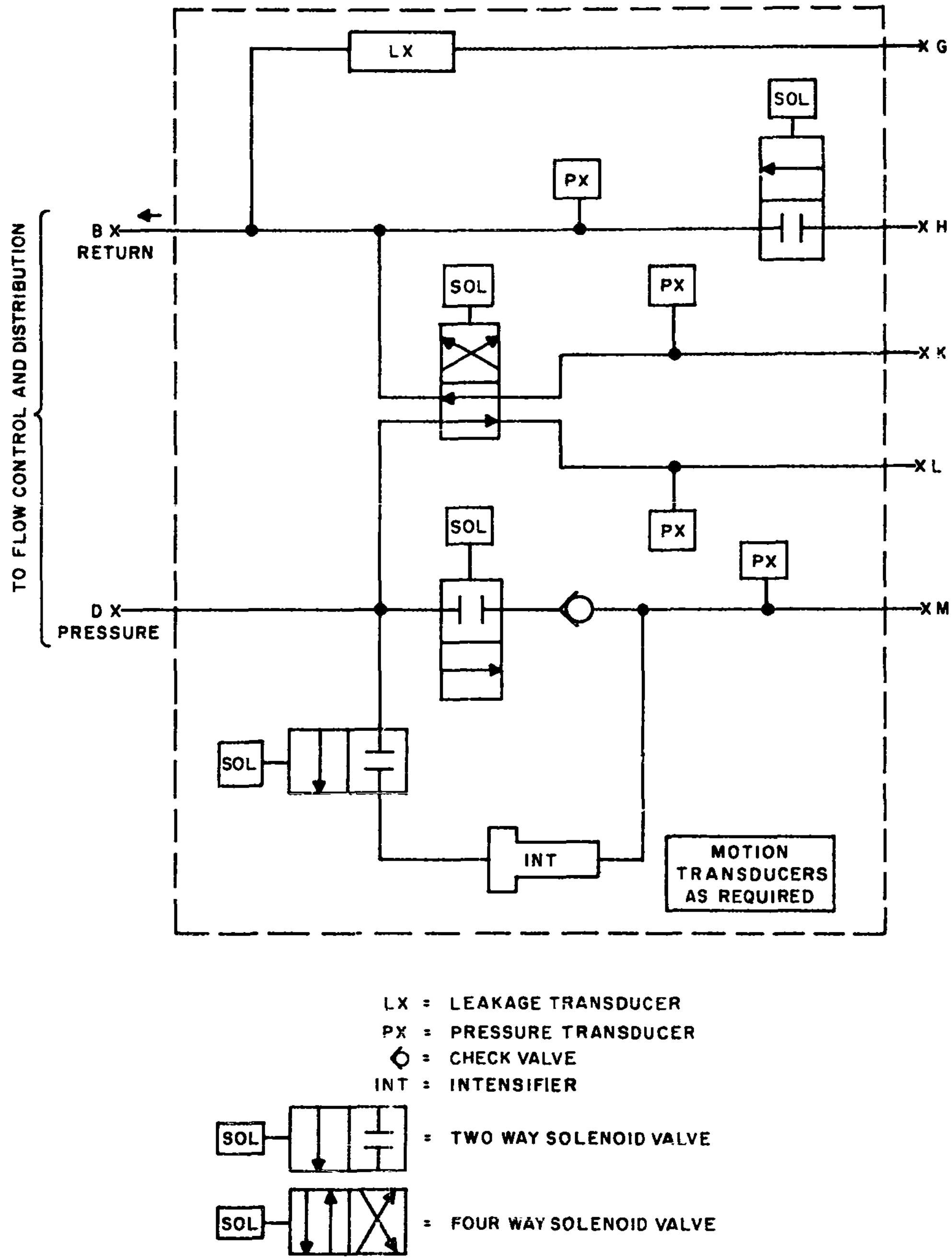


Figure 6-55. Non rotating equipment module - schematic diagram

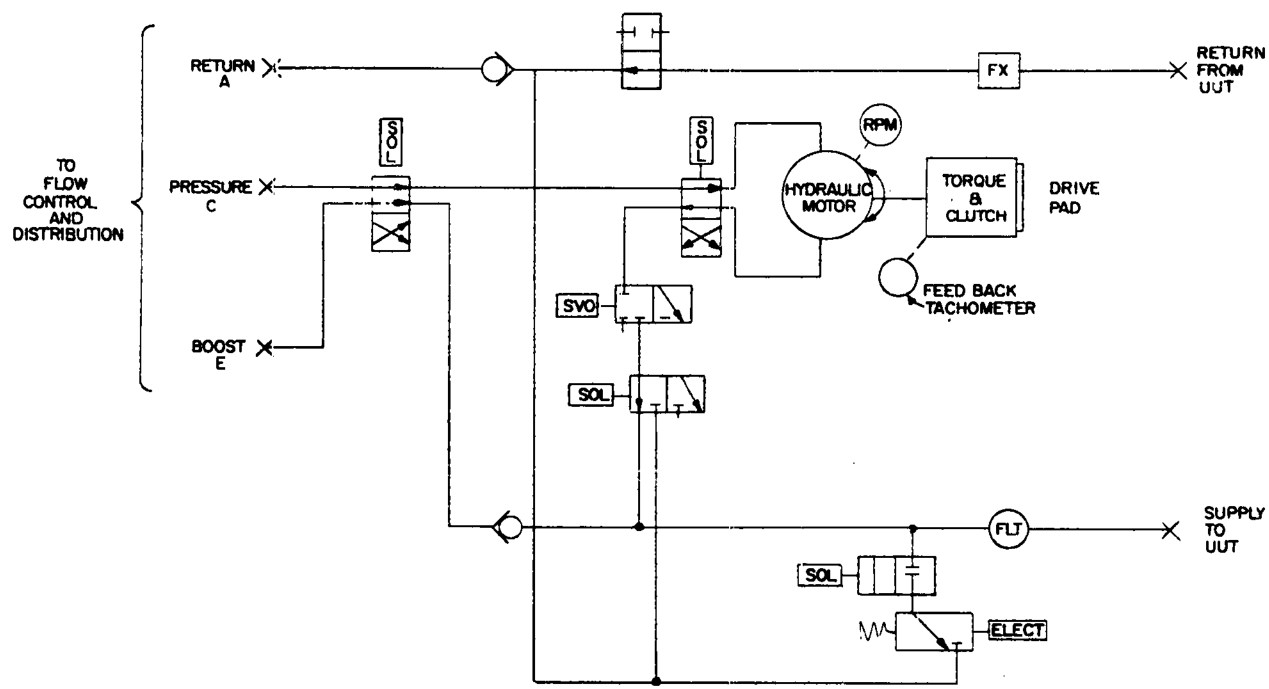


Figure 6-56. Rotating equipment module - schematic diagram

A boost circuit is also included for testing pumps such as provided for the Mauler azimuth turret drive to its maximum flow capability without increasing the requirements of the main pump in the Hydraulic Test Stand.

The physical parameters of this module will be defined when further information is obtained on the commercial motors being considered for this application and when research of rotating components to be tested is further along. It is expected that the major source of noise in the Hydraulic Test Stand will be the hydraulic pumps and motors being tested; however, insulation of these units would impede operator access for adjustment. This area will be completely studied later in the program and every possible attempt will be made to achieve a practical solution.

(v) Filtration (Figure 6-57)

Reservoir Fill - To prevent introduction of contaminants which may be present in the replenishing fluid, the filter system shown in Figure 6-57A is used. The fluid is supplied at port 22, and passes through a filter and selector valve to a circulating pump which directs the fluid through the main filter shown to the reservoir.

Missile System Fill and Cleanout - Flushing of contaminated systems is accomplished with the circuit shown in Figure 6-57B. Port 21 supplies fluid to the contaminated system; the system return is at port 22. Filtered fluid is circulated from the reservoir by means of the pump through the contaminated system. Fluid returning from the contaminated system is filtered before returning to the reservoir.

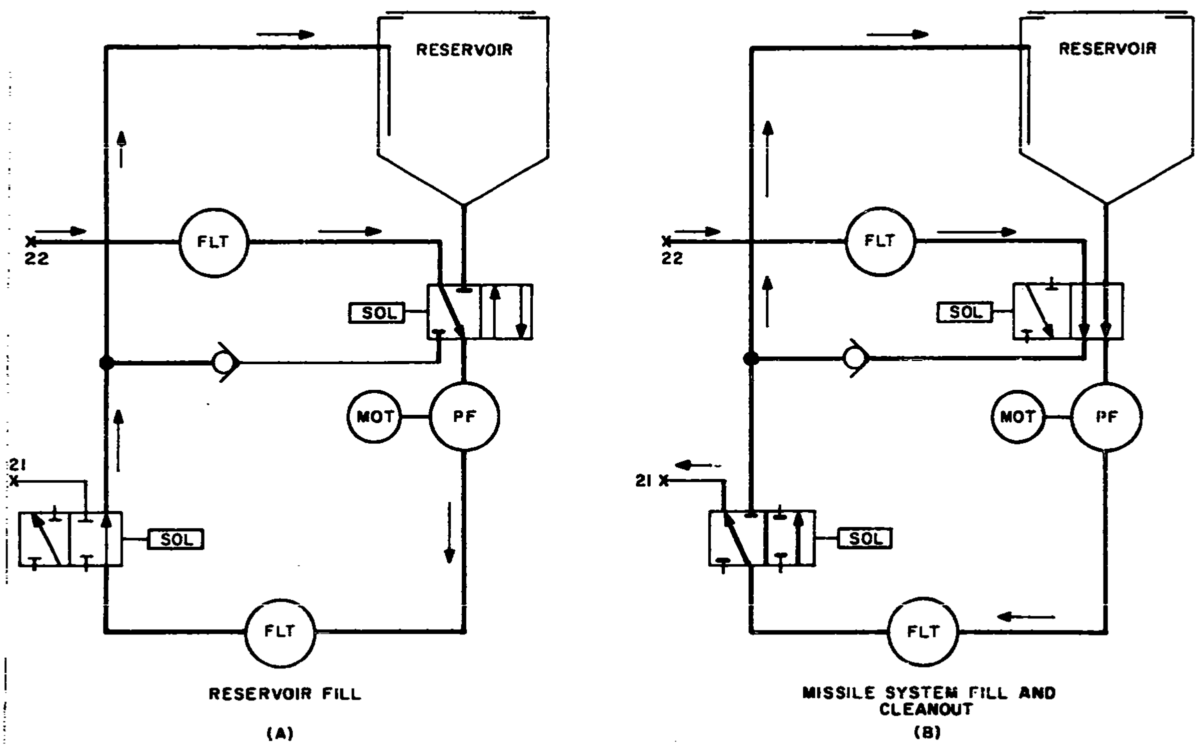


Figure 6-57. Power supply fill and filtering section - schema

1

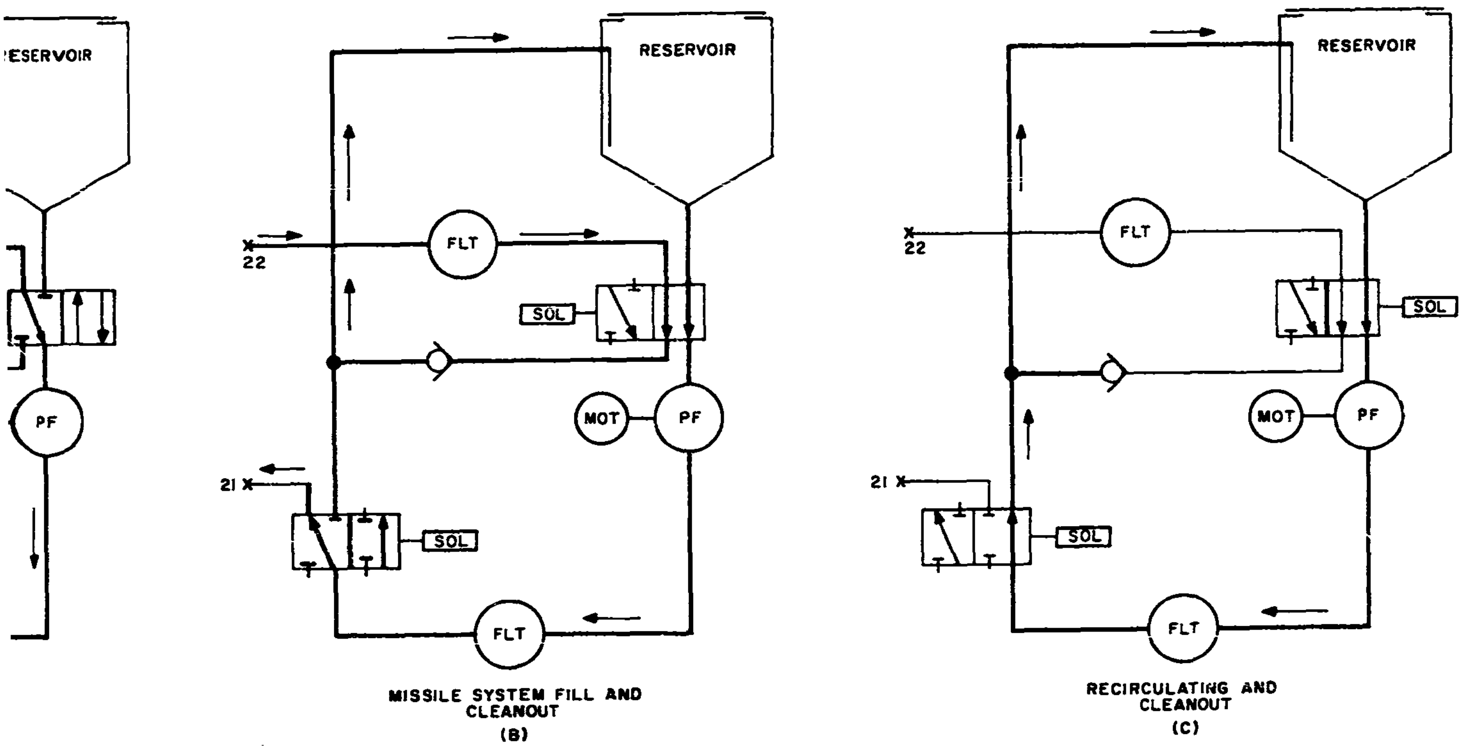


Figure 6-57. Power supply fill and filtering section - schematic diagram

2

Recirculating and Cleanout - The close fits required to produce high pressures in the hydraulic system and the large forces developed lead to the generation of contaminants within the Hydraulic Test Set. Removal of these particles can generally be kept abreast of their generation by standard filtration means. To ensure that a system will remain contaminant free it is necessary to provide filtration at a rate greater than the normal fluid use. Accordingly (see Figure 6-57C) fluid from the reservoir is circulated continuously through a high-capacity filter. This circulation is performed by a low-pressure, high-volume pump which contributes little contamination to the system and does not promote "channeling" through the filters. This pump is separate from the Hydraulic Test Stand main pumping system and provides filtration whether the HTS main pump is utilized or not.

Heat Exchanger - The heat exchanger is expected to present a major space problem. It appears that space considerations prohibit making this component an integral part of the power supply. Consideration is being given to storing the heat exchanger within the console test area for transportation. This unit would be hinged to swing to position outside the shelter when in use. Heat exchanger size has not been determined.

3. Electrical System

To aid in determining the physical parameters of the electrical system, meetings were held with General Electric to present requirements for 400-cycle motors to operate the main pump, boost pump, fan motor, etc. Since size and weight are of primary concern in the Hydraulic Test Set, General Electric has been requested to begin a design study to determine what can be done to conform to the requirements. Some trade-offs may have to be made, but only after a detailed analysis which will include the study of the torque-current curves.

The Hartman Company was also contacted. Requirements were outlined for the type of starting equipment which will be required. A quotation is expected in the near future.

A meeting was held with the Denison Engineering Company to present requirements for servo valves and similar types of equipment contained in a closed loop system.

D. Plans

The Technical Requirements Analysis Report and the Physical Parameters Study Report will be prepared by Greer and submitted by 15 May to RCA for comment. RCA comment will be completed by 30 May. The TRA will be updated at the end of the next quarter.

Design and development effort will begin. This will include the hydraulic, pneumatic, and electrical design.

Construction of the Hydraulic Test Stand breadboard will begin.

Research on test procedures and programs will begin; this will constitute the preliminary groundwork for the establishment of a test program plan which will continue through the development of the Hydraulic/Pneumatic Test Set.

Orientation work on technical manuals and notes on development-type material will begin.

Release of long-lead items will be made.

6.2.3 SERVOVALVE TESTING

The Third Quarterly Interim Technical Report discussed the techniques to be employed in the MTE approach for servovalve testing. To review them briefly, they are as follows:

This type of frequency response (hysteresis) test lends itself well to the MTE concept of automatic testing. The input and output signals take the form shown in Figure 6-58.

The input signals is approximately 5 cps and the phase lag is generally less than 30 degrees for most valves, depending upon the amplitude. For these conditions the elapsed time between t_0 and t_1 (Figure 6-58) is 16 milliseconds. Using the Time Interval and Frequency Meter to measure this time interval (with its time measurements of one count every microsecond), accuracy in phase measurements can approach two thousanths of a degree.

If the frequency response technique of valve testing were not employed, this hysteresis information would have to be derived by a manual test method. The test would be accomplished by first decreasing the differential current from a maximum negative value until the valve output flow reaches zero, and then by decreasing the differential current from a maximum positive value until zero flow is noted. This is shown graphically in Figure 6-59.

6.2.4 INSTALLATION SEQUENCE TESTS

Hydraulic Test Stand installation sequence tests will be made during the next quarter using a dummy loaded Hydraulic Test Stand mockup and the Hydraulic Test Set Shelter mockup. These tests will disclose any Hydraulic Test Stand installation problems.

6.2.5 HYDRAULIC-TEST-SET TEST AND REPAIR CAPABILITIES

A listing of typical hydraulic components is given in Table 6-6, along with the types and causes of failures, and repair and test requirements. This information indicates the high percentage of repairs that can be done in the field (i.e., with the Hydraulic Test Set). This table will be updated to reflect specific UUTs from Mauler and list the specific repairs that can be accomplished on each component.

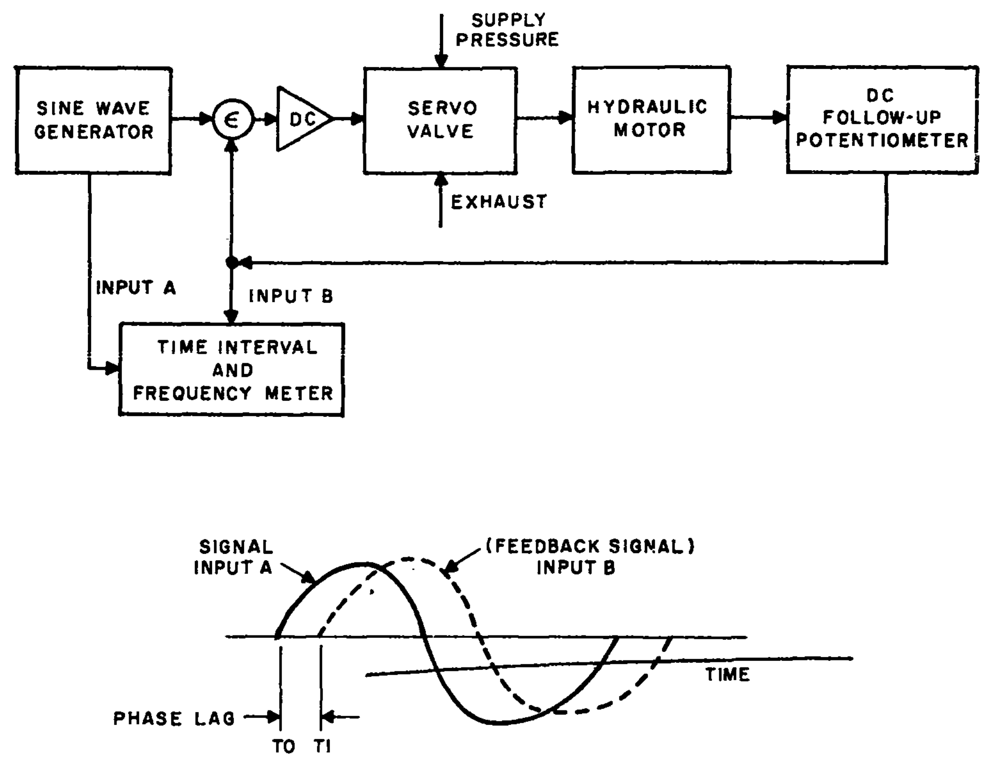


Figure 6-58. Set-up for frequency test of a valve

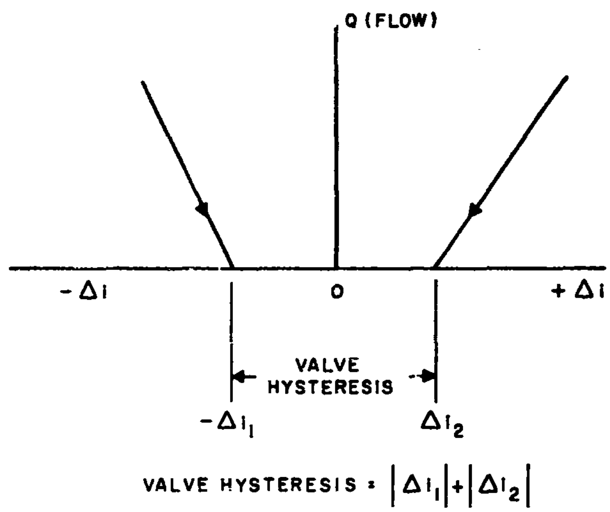


Figure 6-59. Value hysteresis

SECTION 7

SOFTWARE

The objectives of the MTE Software effort are:

(1) development of an Interim Programmer's Guide and establishment of a basic Engineering Programming Process;
(2) preparation of 20 pilot programs to refine and verify programming methods;
(3) preparation of 80 self-test and missile-test programs.

7.1 INTERIM PROGRAMMER'S GUIDE

7.1.1 PROGRESS

A preliminary plan and schedule for the writing and assembly of an Interim Programmer's Guide was developed based on previously prepared outlines. Plans and outlines are being re-evaluated as a result of: (1) development of philosophy of scope of the Guide, and (2) techniques being developed in establishing a basic Engineering Programming Process.

The first draft of the computer portion of the Guide has been completed, and the controller instruction complement defined. The switching control language, completed subject to verification and revision, is included in Appendix B.1 of this report.

A series of switching control charts has been prepared as a working tool for the pilot programming effort; these charts list each stimulus and measurement subsystem along with its respective ranges, sub-modes, switching-word formats, least increments and, where available, timing and accuracy.

7.1.2 STATUS (4 April 1963)

Work is concentrated in Computer/Controller programming and switching control. The computer portion of the Programmer's Guide is being reviewed.

7.1.3 PLANS FOR NEXT QUARTER

(1) Develop detailed requirements for the Interim Programmer's Guide.
(2) Continue preparation of guide material for the pilot programming effort.
(3) Complete draft copy of the Interim Programmer's Guide.

7.2 PILOT PROGRAMS

7.2.1 PROGRESS

The results and recommendations of the Computer Programming Study Report (Report No. CR-62-547-14, dated 6 September 1962) were reviewed. A program plan was developed for instrumenting an Engineering Programming Process for preparation of the 20 pilot programs.

A Preliminary Test Procedure specification was developed to establish a simple, compatible, standard interface between test-design engineering and the programming function. The Test Procedure specification defines the requirements for the form and content of the following items:

(1) Title and Revision Sheet
(2) Introduction
(3) Test Design
(4) Equipment Required
(5) Preparation for Test
(6) Operational Procedure
(7) Test Detail

A programming chart was prepared as a tool for the preparation of Test Procedures. This chart delineates, in readily accessible tabular form, all the

possible switching configurations, and the available timing and tolerance constraints necessary to the completion of a test procedure.

An MTE Symbolic Coding Form was designed for assembly and coding of: (1) data from the test procedure, and (2) the necessary logical control of MTE in pseudo language.

The following UUTs were selected for the Pilot Programming effort:

System	Govt. Spec. or Ord. No.	UUT Type
Hercules	G.S. 17747	±320V Power Supply
Hercules	G.S. 17622	Electronic Control Amplifier
Hercules	G.S. 153846	DC Amplifier
Ajax	G.S. 58678	Interval Timer
Hawk	9189402 or 9195808	AFC and Decoder Assy.
Acquisition Radar	10091073	Receiver, Main IF
Acquision Radar	10090042	Synchronizer, Electric
Gate, TI, Radar	10091420	Speedgate Assembly
Turret Pod Assembly	1076914	Azimuth Servo Hydraulic Valve
Track Eval. Computer	10096704	Arithmetic Unit Assembly No. 1
Internal Power Supplies	MTE 5753	9 VDC Power Supply
DC Stimulus	MTE 5808	0-9.99 VDC, 10 V Ref., Stimulus
High Frequency Stimulus	MTE 5853	If Processer
High Frequency Stimulus	MTE 5844	X-Band Ratiometer
Low Frequency Stimulus	MTE 5738	Frequency Standard
Low Frequency Stimulus	MTE 5733	VLF Generator
Measurements	MTE 5782	Data Output Buffer
Measurements	MTE 5779A	Monitor Adapter
Computer/Controller	MTE 5887	Comparator-Time Delay
Computer/Controller	MTE 5811	Arithmetic

The first pilot UUT program is being processed.

7.2.2 STATUS (1 April 1963)

Test procedure development has started for the first of 20 pilot programs; the first UUT, Number 0001, is the Hercules, GS 17747, Power Supply.

7.2.3 PLANS FOR NEXT QUARTER

(1) Design utility programs as required by the pilot programming effort. These include input-output service routines and routines common to all programs.
(2) Continue refinement of the Engineering Programming Process as a result of experience gained in the pilot programming effort.
(3) Complete 12 pilot programs in assembly-level language (pseudo language).
(4) Start the translation of programming or pseudo language to absolute or machine language, to ready the pilot programs for operational use.

7.3 SELF-TEST AND MISSILE TEST PROGRAMS

7.3.1 PROGRESS

A program plan was developed for the preparation of 80 self-test and missile test programs. The following self-test programs have been identified:

HTS Controller
Measurement Integration
DC Stimulus Integration
LF Stimulus Integration
HPU Integration
Systems Test
Acceptance Test

ETS Computer-Controller
Measurement Integration
DC Stimulus Integration
LF Stimulus Integration
HF Stimulus Integration

System Test

Acceptance Test

7.3.2 STATUS (1 April 1963)

A preliminary program plan exists in PERT Logic, Self-test Programs are identified.

7.3.3 PLANS FOR NEXT QUARTER

Identify the remaining 66 UUTs. Start self-test programming effort.

7.4 SUPPORT PROGRAM

7.4.1 PLANS FOR NEXT QUARTER

Start design activity on a support program for preparation of magnetic tapes in MTE standard cartridges. MTE test programs will be translated from Hallerith cards or paper tapes to the standard cartridge. Equipment involved will be a support computer (such as the RCA 301 class), MTE magnetic tape transport, and necessary hardware.

SECTION 8

PRODUCT ASSURANCE

8.1 PROGRESS

8.1.1 RELIABILITY

A. Reliability Estimates for MTE Sets

The initial reliability goal for the MTE system was 500 hours. TDO MTE-12 then set the goal of 500 hours each for the Electronic Test Set and the Hydraulic Test Set. RCA recommended in reply to TDO MTE-12 that more realistic goals of 50 hours for the Electronic Test Set and 250 hours for the Hydraulic Test Set be established. These goals are apportioned in Tables 8-2 and 8-4 to the MTE specification box level (i. e., MTE 5848). These are preliminary goals based on information currently available. These goals will be constantly compared with the predicted values to insure that the goals for the sets are attained. As finalized design data becomes available the individual goals may have to be adjusted. The primary concern, however, is to meet the overall system goal of 50 hours for the Electronic Test Set.

a. Electronic Test Set

The reliability estimate for the Electronic Test Set is based on the latest system configuration per RCA Drawing 1734187, Revision B, dated 1 March 1963. Table 8-1 summarizes the results for Electronic Test Groups 1 and 2. Based on a serial model, the calculated MTBF for the Electronic Test Set is 41.5 hours. Table 8-2 is a detailed breakdown, per MTE Specification, for the Electronic Test Set. The calculated values of failure rate can still be considered preliminary data and will be updated as finalized data becomes available. The majority of failure rates were calculated for 10% electrical stress and 25°C ambient temperature.

Table 8-1. Summary of reliability estimate for ETS

ELECTRONIC TEST SET		Present Pred. Failure Rate %/1000 hr.	Apportioned Goal %/1000 hr.	Apportioned Goal MTBF Hrs.
ETG - 1		1857.645	1554.00	64.3
5896	Tape Transport	41.086	35.00	2857
5716	High Frequency Stimulus Unit No. 2	373.490	312.00	320.5
	High Frequency Stimulus Unit No. 1	676.393	565.00	177.0
5846	X Band Load	1.500	1.50	66700
5852	L Band Load	1.500	1.50	66700
5869	Operator Console Unit	271.152	227.00	441
5714	Measurement Unit	122.208	102.00	980
5713	Comp/Cont. Unit	370.316	310.00	322.6
ETG - 2		560.280	446.00	224.0
5715	Low Frequency Stimulus No. 2	226.757	180.00	555.5
	Low Frequency Stimulus No. 1	150.817	119.50	836
5719	DC Stimulus Unit	168.411	133.50	749.1
5718	Int. Power Supply No. 1	6.625	6.00	16,667
	Int. Power Supply No. 2	7.670	7.00	1429

Predicted failure rate for ETS = 1857.645 + 560.280 = 2417.925 %/1000 hr.

Predicted MTBF for ETS = 41.5 hours

Table 8-2. Detail reliability estimate for ETS

ETG-1		Present Failure Rate %/1000 hr.	Goal %/1000 hr.	Goal MTBF Hrs.
5896	Tape Transport	(Total) 41.086	35.00	2,857
	5840 Circuit Breaker Disconnect	0.340	0.34	294,000
	5741 Level Detector & Atten.	22.710	19.30	5,181
	5813 Tape Transport	10.518	6.43	15,552
	5816 Tape Reader	7.518	8.93	11,198
5716	High Frequency Stimulus	(Total) 1049.883		
	Unit No. 1	676.393	565.00	177
	5892 Breaker Disconn. & Reg.	* 4.500	* 4.50	22,222
	5844 X Band Ratiometer	210.487	177.00	565
	5845 X Band Conversion	137.747	115.00	870
	5843 X Band In/Out	264.503	219.00	457
	5850 L Band Conversion	35.800	30.00	3,333
	5851 L Band Input/Output	23.356	19.50	5,128
	Unit No. 2	373.490	312.00	320.5
	5840 Circuit Breaker Disconnect	0.340	0.34	294,000
	5862 Junction Box	40.664	34.00	2,941
	5858 TWT P/S	16.000	13.30	77,519
	5847 X Band Extender	133.032	111.31	898
	5842 Microwave Synthesizer	35.770	29.90	3,344
	5849 L Band Extender	61.600	51.40	1,946
	5848 Frequency Synthesizer	70.201	58.50	1,709
	5853 I.F. Processing	15.883	13.25	7,547

* Best estimate - (control panel only)

Table 8-2. Detailed reliability estimate for ETS (cont'd)

ETG-I			Present Failure Rate %/1000 hr.	Goal %/1000 hr.	Goal MTBF Hrs.
5846		X Band Load	1.500	1.50	66,700
5852		L Band Load	1.500	1.50	66,700
5869		Operator Console Unit	(Total) 271.152	227.00	441.0
	5876	Visual Instructor	* 15.000	12.50	8,000
	5815	Printer			
	5873	Manual Input	2.316	2.30	43,478
	5745	Message Generator	24.616	20.60	4,854
	5776	Message Receiver	21.354	17.80	5,618
	5896	Mauler Synchronizer	* 6.000	5.00	20,000
	5874	Test Results	* 20.000	16.70	5,988
	5870	Control Panel	20.056	16.70	5,988
	5877	Rack Monitor	* 15.000	12.50	8,000
	5871	Maintenance Panel	27.672	23.10	4,329
	5779A	Monitor Adapter	40.060	33.60	2,976
	5779B	Monitor Adapter	40.060	33.60	2,976
	5891	HF Monitor	* 15.000	12.50	8,000
	5747	Power Loads DC/AF SW	24.018	20.10	4,975

* Best estimate - (control panel only)

Table 8-2. Detailed reliability estimate for ETS (cont'd)

ETG-2			Present Failure Rate %/1000 hr.	Goal 5/1000 hr	Goal MTBF Hr.
		Low Frequency Stimulus	(Total) 377.574		
5715		Low Frequency Stimulus No. 1	150.817	119.50	836.0
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5886	Regulator	4.091	3.36	29,761
	5894	L. F. Stimulus Routing Assembly	* 22.00	17.50	5,714
	5735A	AF/RF Generator 100	69.774	55.00	1,818
	5735B	AF/RF Generator 100			
	5731	Phase Converter	28.761	22.80	4,386
	5758	3 Phase PC P. S. 400	25.851	20.50	4,878
5715		Low Frequency Stimulus No. 2	(Total) 226.757	180.00	555.5
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5886	Regulator	4.091	3.36	29,761
	5736A	RF Synthesizer	36.925	29.40	3,401
	5736B	RF Synthesizer	30.032	24.00	4,167
	5738	Frequency Standard	3.321	2.65	37,735
	5744	Pulse Amplifier	21.608	17.30	5,780
	5743	Pulse Generator	61.608	49.10	2,037
	5733	VLF Generator	67.452	53.80	1,859
	5854	3 AC P. S. 800	1.300	1.05	95,238

*Best estimate - (control panel only)

Table 8-2. Detailed reliability estimate for ETS (cont'd)

ETG - I			Present Failure Rate %/100 hr.	Goal %/100 hr.	Goal MTBF Hrs.
5714		Measurement Unit	(Total) 122.208	102.00	980.4
	5840	Circuit Breaker Disconnect	0.340	0.34	294,000
	5781	Stds & Self-Test Monitor	19.570	16.40	6,098
	5886	Regulator	4.091	3.36	29,761
	5785	Analog Adapter	13.240	11.10	9,009
	5778	Digital Multimeter	17.758	14.90	6,711
	5777	Tifcon	22.433	18.80	5,319
	5782	Data Output Buffer	44.776	37.10	2,695
5713		Computer/Controller Unit	(Total) 370.316	310.00	322.6
	5840	Circuit Breaker Disconnect	0.340	0.34	294,000
	5886	Regulator	4.091	3.36	29,761
	5837	Memory	113.516	94.70	1,056
	5809	Input/Output	13.099	11.00	9,091
	5836	Control Unit	29.579	24.70	4,049
	5811	Arithmetic Unit	39.027	32.70	3,058
	5812	Switching Control Buffer	45.884	38.50	2,597
	5887	Comparator/Tape Search	* 39.000	32.70	3,058
	5810	Control Director	49.780	41.80	2,392
	5889	Peripheral Control	* 36.000	30.20	3,311

* Best estimate - (control panel only)

Table 8-2. Detailed reliability estimate for ETS (cont'd)

ETG-2			Present Failure Rate %/1000 hr.	Goal %/1000 hr.	Goal MTBF Hrs.
5719		DC Stimulus Unit	(Total) 168.411	133.50	749.1
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5886	Regulator	4.091	3.36	29,761
	5752	280-2850 VDC P. S.	23.161	18.30	5,464
	5751	20-300 VDC P. S.	29.594	23.50	4,255
	5750	0-36 VDC P. S.	22.245	17.60	5,682
	5750	0-36 VDC P. S.	22.245	17.60	5,682
	5750	0-36 VDC P. S.	22.245	17.60	5,682
	5750	0-36 VDC P. S.	22.245	17.60	5,682
	5750	0-36 VDC P. S.	22.245	17.60	5,682
5718		Internal Power Supply Unit No. 1	(Total) 6.625	6.00	16,667
	5840	Circuit Breaker Disconnect	.340	0.33	294,000
	5753	12 VDC P. S.	.825	0.75	133,333
	5753	12 VDC P. S.	.825	0.75	133,333
	5753	12 VDC P. S.	.825	0.75	133,333
5718	5755	18 VDC P. S.	.635	0.57	175,430
	5755	18 VDC P. S.	.635	0.57	175,430
	5755	18 VDC P. S.	.635	0.57	175,430
	5755	18 VDC P. S.	.635	0.57	175,430
	5755	18 VDC P. S.	.635	0.57	175,430
	5755	18 VDC P. S.	.635	0.57	175,430

Table 8-2. Detailed reliability estimate for ETS (cont'd)

			Present Failure Rate %/1000 hr.	Goal $ %/1000 hr.	Goal MTBF Hr.
5718		Internal Power Supply Unit No. 2	(Total) 7.670	7.0	1429.0
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5757	120 VDC P.S.	1.360	1.24	80,645
	5757	120 VDC P.S.	1.360	1.24	80,645
	5754	60 VDC P.S.	1.300	1.19	84,033
	5754	60 VDC P.S.	1.300	1.19	84,033
	5756	30 VDC P.S.	.670	0.60	166,666
	5756	30 VDC P.S.	.670	0.60	166,666
	5756	30 VDC P.S.	.670	0.60	166,666

b. Hydraulic Test Set

A preliminary reliability estimate was also prepared in a similar manner for the Hydraulic Test Set, i e., 10% stress and 25°C. These results are presented in Tables 8-3 and 8-4, summary and detailed breakdowns, respectively. The current predicted MTBF for the Hydraulic Test Set is 171 hours, whereas RCA's recommended design goal was set at 250 hours in the RCA reply to TDO MTE-12. These goals may have to be adjusted as final design data becomes available.

B. System Availability

In reply to TDO MTE-12 regarding a change in the MTE reliability goal, Design Product Assurance performed an analysis to evaluate the influence of MTBF on equipment availability. This analysis encompassed the following factors: MTBF, Mean Down Time, Number of UUT's tested per day, UUT Test Time, and Available Test Time per day.

The above factors are related by the following equation:

$$N = \left(\frac{MTBF}{\bar{M}_t + MTBF}\right) \left(\frac{T_1}{T_2}\right) (\text{Accuracy}) \qquad (1)$$

Where:

N = Number of UUT's tested per day (average)
MTBF = Mean Time Between Failure

Table 8-3. Summary of reliability for Hydraulic Test Set

		Present Failure Rate %/1000 hr.	Goal %/1000 hr.	Goal MTBF hr.
Hydraulic Test Set (5702)		584.980	400	250
5722	Hydraulic Test Stand	74.160	50.78	1969
5720	Measurement Unit	162.268	111.00	900.9
5885	Operator Control Console	74.834	51.40	1953
5723	Swing Out Pneumatic Pump	* 10.00	6.84	14620
5719/5721	Controller Stimulus Unit	259.063	177.00	564.9
5724	Internal Power Supply Unit	4.655	3.18	31447

Present MTBF for HTS = 171.0 hours

* Best estimate - (control panel only)

Table 8-4. Detailed reliability estimate for Hydraulic Test Set

Hydraulic Test Set (5702)			Present Predicted Failure Rate %/1000 hrs.	Goal %/1000 hrs.	Goal MTBF Hrs.
5722		Hydraulic Test Stand	74.160	50.78	1,969
5720		Measurement Unit	(Total) 162.268	111.00	900.9
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5781	Standard & Self Test	19.570	13.40	7,463
	5886	Regulator	4.091	2.74	36,496
	5779A	Monitor Adapter	40.060	27.40	3,650
	5779B	Monitor Adapter			
	5785	Analog Adapter	13.240	9.12	10,965
	5778	Digital Multimeter	17.758	12.10	8,264
	5777	Tifcon	22.433	15.30	6,536
	5782	Data Output/Buffer	44.776	30.60	3,268
5885		Operator Control Console Unit	(Total) 74.834	51.20	1,953
	5876	Visual Instructor	* 15.000	10.16	9,843
	5815	Printer			
	5873	Manual Input	2.316	1.68	59,524
	5816	Tape Reader	7.518	5.24	19,084
	5874	Measured Value Display	* 20.000	13.60	7,353

* Best estimate - (control panel only)

Table 8-4. Detailed reliability estimate for Hydraulic Test Set (cont'd)

Hydraulic Test Set (5702)			Present Predicted Failure Rate %/1000 hrs.	goal %/1000 hrs.	Goal MTBF Hrs.
	5883	Control Panel	* 10.00	6.84	14,620
	5893	Rack Monitor	* 10.00	6.84	14,620
	5884	Maint. Panel	* 10.00	6.84	14,620
5723		Swing Out Pneumatic Pump	10.00	6.84	14,620
5719/ 5721		Controller Stimulus Unit	(Total) 259.063	177.00	564.9
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5812	Switch Control Buffer	45.884	31.30	3,195
	5887	Tape Search to Digital Comp.	* 39.00	26.67	3,750
	5810	Control Director	49.780	34.00	2,941
	5889	Peripheral Control	* 36.00	24.60	4,065
	5886	Regulator	4.091	2.74	36,496
	5750	0-36 VDC P.S.	22.245	15.20	6,579
	5750	0-36 VDC P.S.	22.245	15.20	6,579
	5808	0-10 VDC P.S.	26.356	18.00	5,556
	5857	115 & 10 VAC P.S.	13.122	8.95	11,173

* Best estimate - (control panel only)

Table 8-4. Detailed reliability estimate for Hydraulic Test Set (cont'd)

Hydraulic Test Set			Present Predicted Failure Rate %/1000 hr.	Goal %/1000 hr	Goal MTBF Hrs.
5724		Internal Power Supply Unit	(Total) 4.655	3.18	31,447
	5840	Circuit Breaker Disconnect	.340	0.34	294,000
	5757	120 VDC P. S.	1.360	0.92	108,696
	5756	30 VDC P. S.	.670	0.44	227,273
	5755	18 VDC P. S.	.635	0.42	238,095
	5753	12 VDC P. S.	.825	0.53	188,679
	5753	12 VDC P. S.	.825	0.53	188,679

Where:

M_t = Mean Down Time = 1.76 (including preventive maintenace) hours

T_1 = Available Test Time, hours

T_2 = Time to Test UUT = 0.5 hours for ETS = 1.0 hours for HTS

Accuracy = 0.999 (The probability that the MTE System will not make an error in classifying a UUT as good or bad.)

Substituting the above values into Equation (1) gives

For the Electronic Test Set

$$N = \frac{1.998\ T_1\ (MTBF)}{MTBF + 1.76} \qquad (2)$$

For the Hydraulic Test Set

$$N = \frac{0.999\ T_1\ (MTBF)}{MTBF + 1.76} \qquad (3)$$

Equations 2 and 3 are plotted in each of Figures 8-1 and 8-2 for two values of T_1, the available test time. It is seen that RCA's proposed goals of 50 hours for the Electronic Test Set and 250 hours for the Hydraulic Test Set are past the knee of the curve where increasing the MTBF does not provide an appreciable increase in the number of UUT's that can be tested per day. This conclusion can be examined more closely by solving equation 1 for MTBF. The result is:

$$MTBF = \frac{N\ (T_2/T_1)\ \bar{M}_t}{0.999 - N\ (T_2/T_1)} \qquad (4)$$

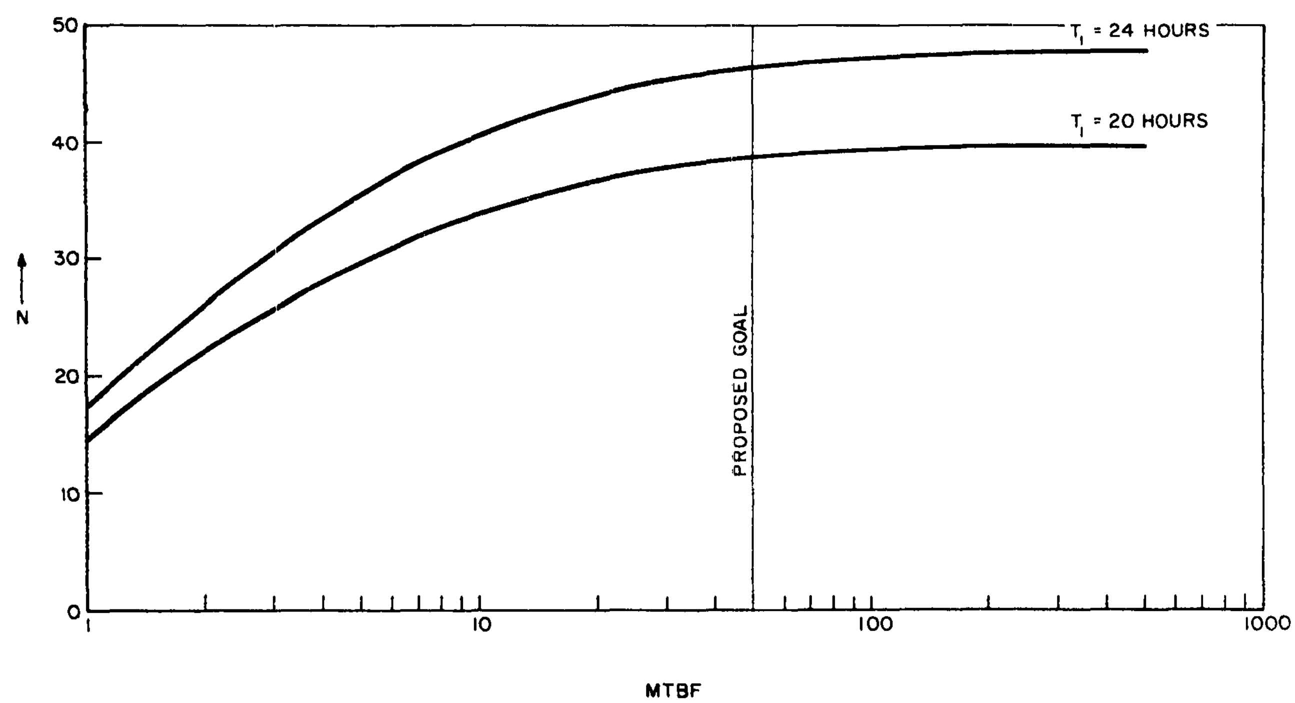


Figure 8-1. MTBF vs. No. of UUTs tested per day

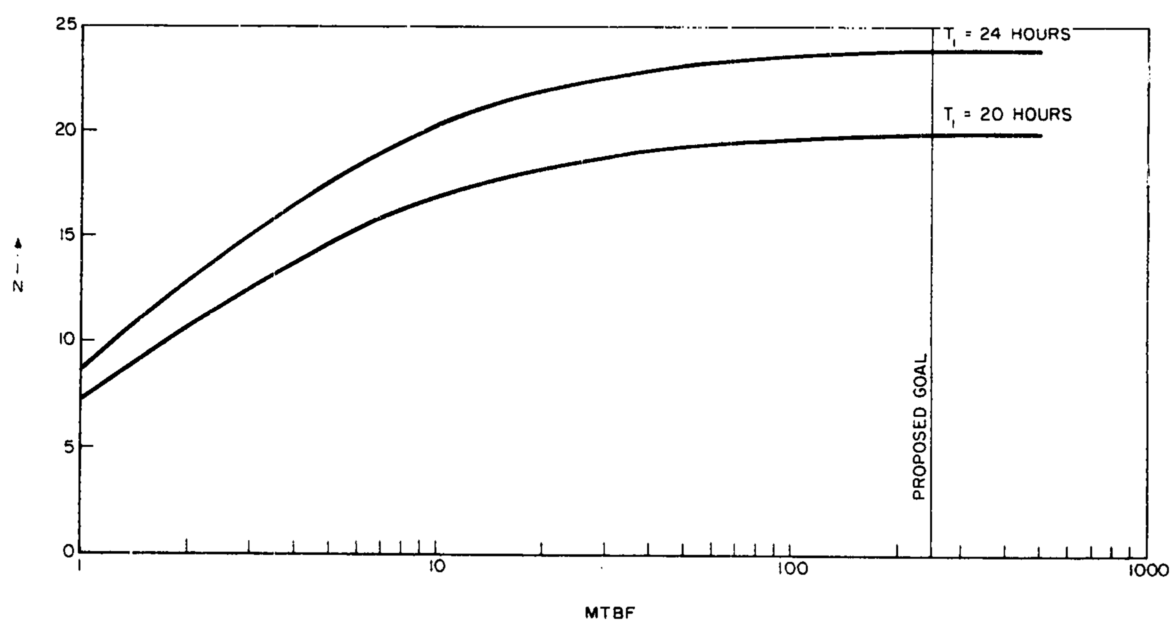


Figure 8-2. Hydraulic/Pneumatic test set - MTBF vs. No. of

Thus,

$$MTBF \rightarrow \infty$$

when

$$\left[0.999 - N(T_2/T_1)\right] \longrightarrow 0.$$

This is defined as the limiting boundary, beyond which no more additional UUT's can be tested even if the MTBF is increased. Solving

$$0.999 - N\ (T_2/T_1) = 0 \qquad (5)$$

For N gives

$$N = 0.999 \left(\frac{T_1}{T_2}\right) \qquad (6)$$

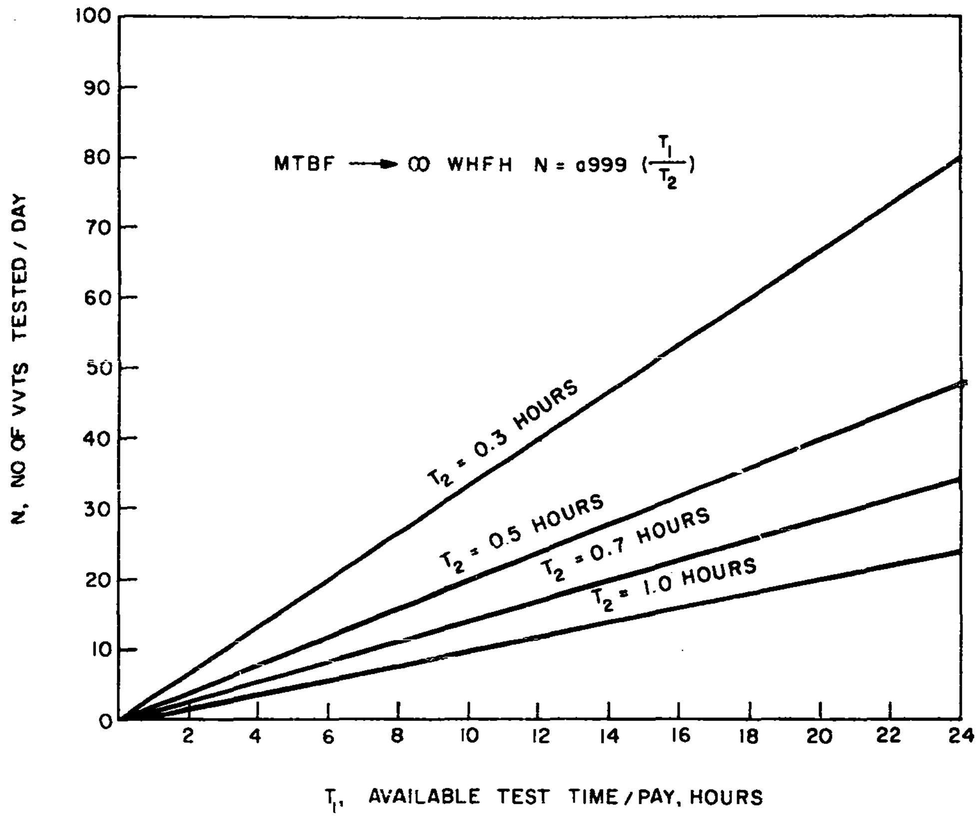
This equation is plotted in Figure 8-3 for various values of T_1 and T_2. These curves also indicate the increased number of UUT's that can be tested per day if the UUT test time is decreased.

C. Redundancy Studies

Design Product Assurance has performed a redundancy study based on the present system configuration. The type of redundancy studies is standby with repair. The equivalent failure rate, λeq., for this type redundancy is:

$$\lambda\ eq = \frac{\lambda 2}{2\lambda + u}$$

Where: λ is in failures per hour and u is the repair rate in units per hour. For this study, it was assumed that the repair rate is constant for each unit at one per hour, and that the switching and fault sensing reliability was one.



NOTE: CURVES APPLICABLE TO BOTH ELECTRONIC TEST SET AND HYDRAULIC / PNEUMATIC TEST SET

Figure 8-3. Limiting boundary curves

It is seen that unit standby redundancy is more effective than making an entire system redundant. It must be emphasized again that switching and fault sensing reliability will decrease unit redundancy appreciably.

D. Detailed Stress Analysis

The MTE Program is currently entering a phase where detailed finalized information is becoming available; and hence, stress analyses can be made to the part level, on all units. Tables 8-6 and 8-7 present the failure rates, per standard millimod, at 25°C and 60°C, respectively, on circuits conducted to date.

In addition to the standard millimods, stress analyses are being performed on the internal power supplies. These results are incomplete at this time, but will be reported on in the next quarterly.

It is to be emphasized that switching and fault sensing reliability can drastically reduce the overall MTBF.

The results of this study are shown in Figures 8-4, 8-5, and 8-6 for Electronic Test Groups 1 and 2 and the Hydraulic Test Set respectively. Figures 8-7, 8-8, and 8-9 are the models used for Figures 8-4, 8-5, and 8-6. The failure rates used were the ones given in Tables 8-1 and 8-3. The unit with the highest failure rate was made redundant first, then the next highest one, and so forth until all units are in redundancy.

A comparison was then made between unit redundancy and system redundancy. The unit redundancy models used are as follows:

ETG No. 1	Model 7	Figure 8-7
ETG No. 2	Model 4	Figure 8-8
HTS	Model 6	Figure 8-9

The system redundancy models used are given in Figure 8-10.

The results of this study are presented in Table 8-5.

Table 8-5. Redundancy study results

	MTBF (Hours)		
	Goals	Entire System in Standby Redundancy (Figure 8-5)	All Units in Individual Standby Redundancy (Figures 8-7, 8-8 and 8-9)
ETG - 1	64.3*	3010	12100
ETG - 2	224*	32300	110000
HTS	250	29800	96200

* Based on 50 hour goal for Electronic Test Set

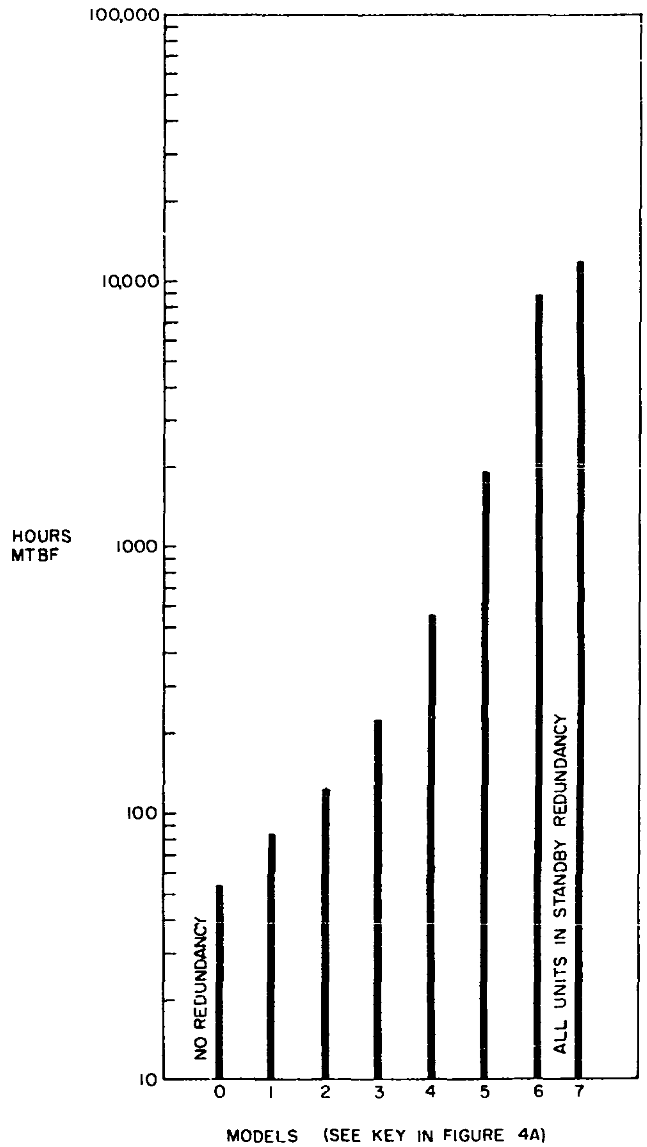


Figure 3-4. Standby redundancy with repair for electronic test group No. 1

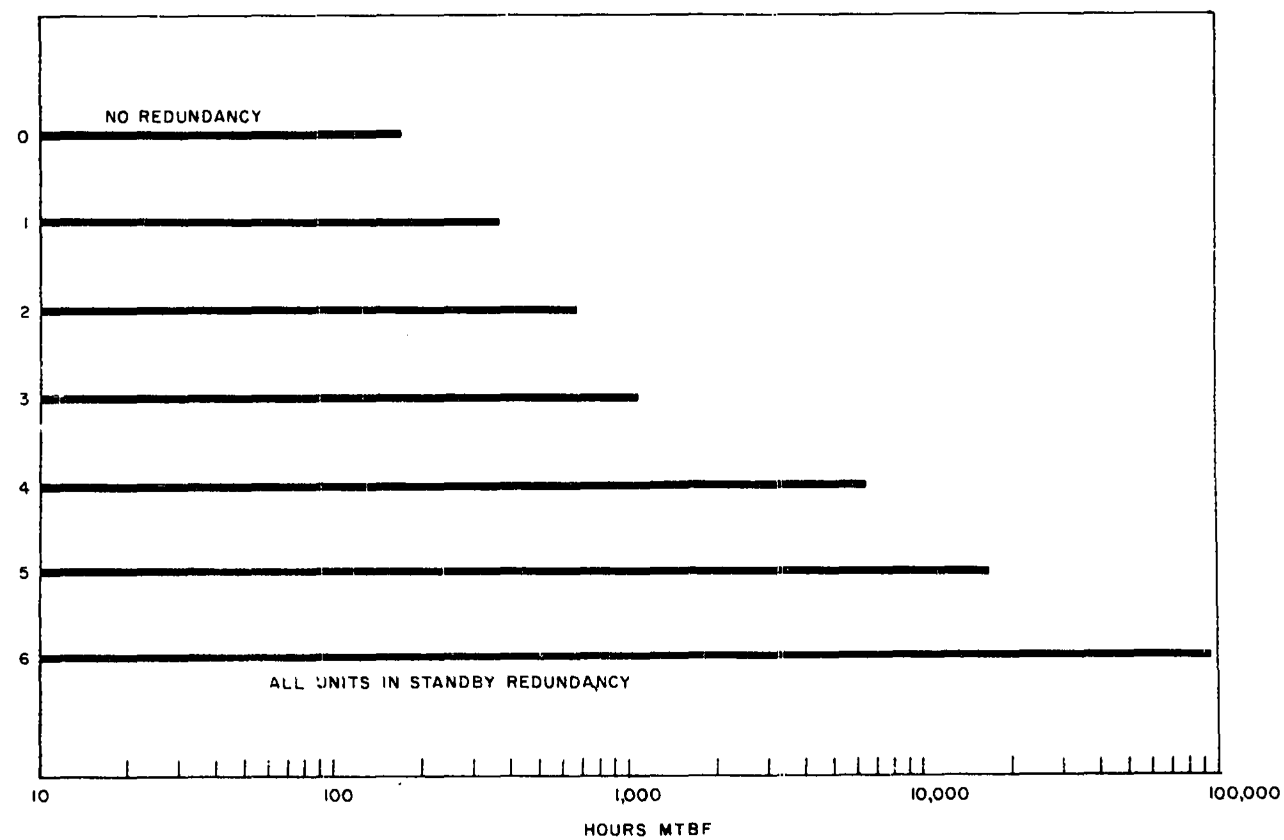


Figure 8-5. Standby redundancy with repair for electronic test group No. 2

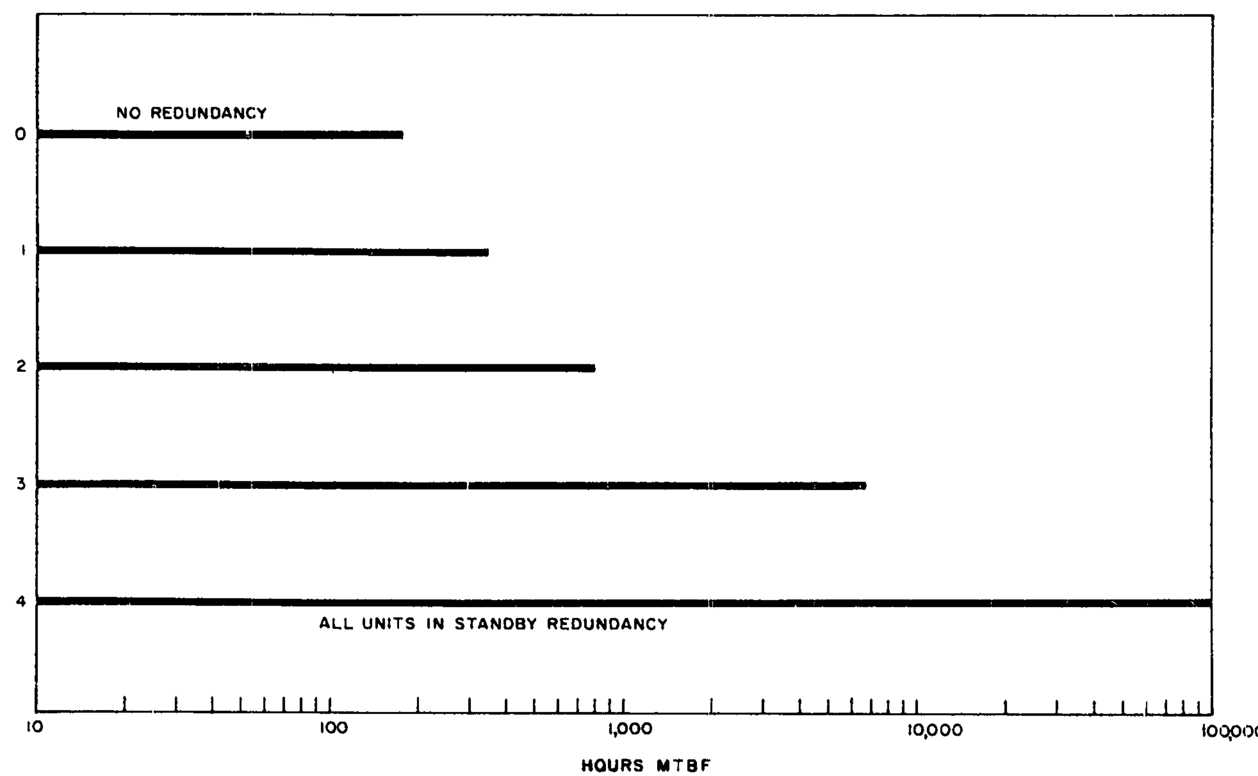


Figure 8-6. Standby with repair for hydraulic/pneumatic test set

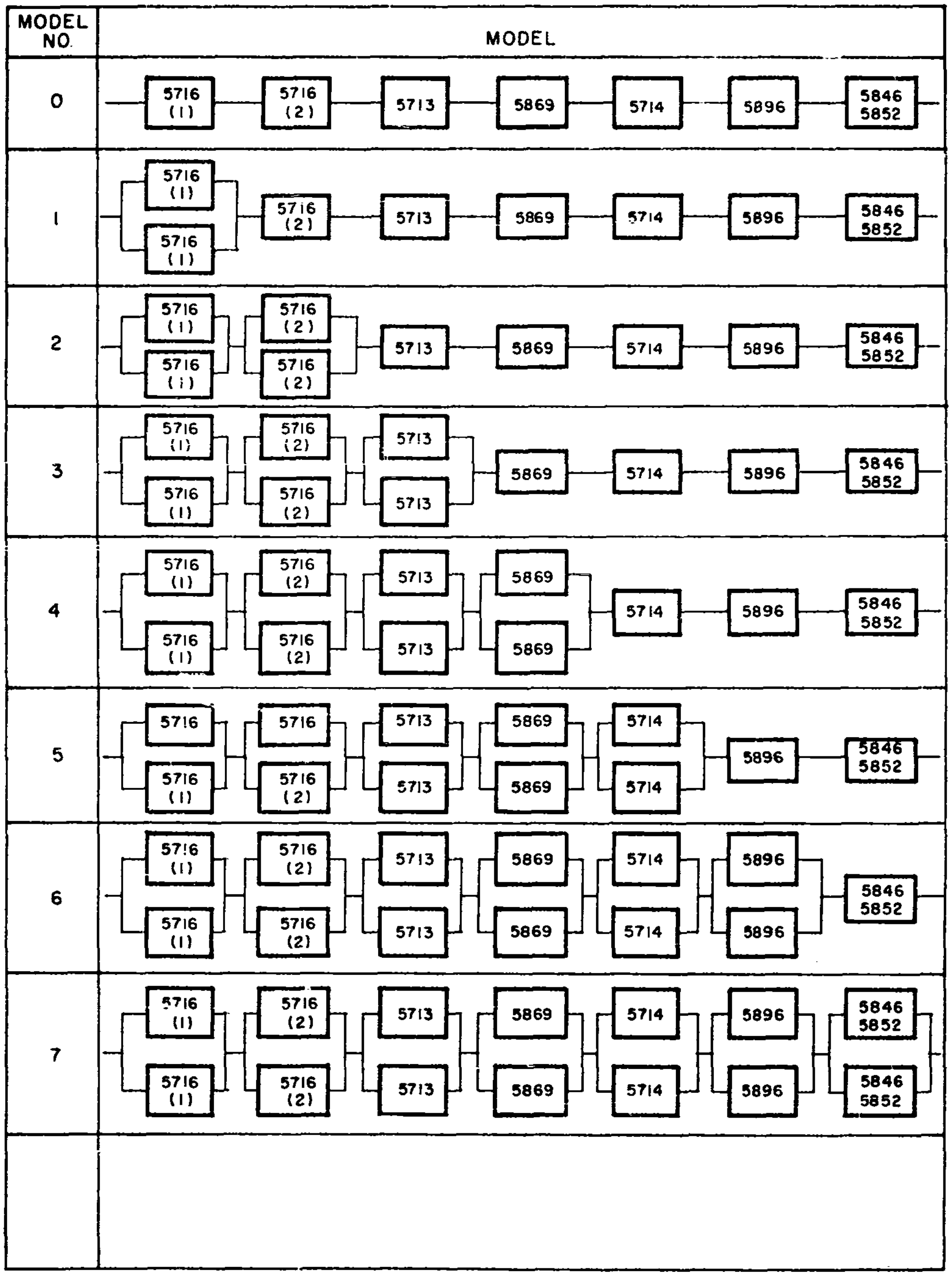


Figure 8-7. Models used for electronic test group No. 1

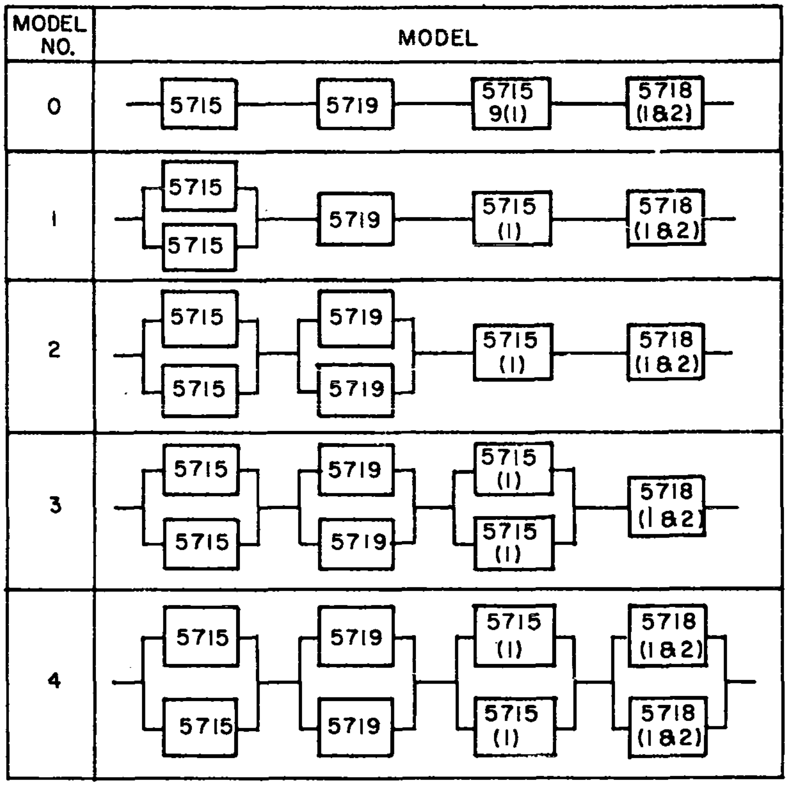


Figure 8-8. Models used for electronic test group No. 2

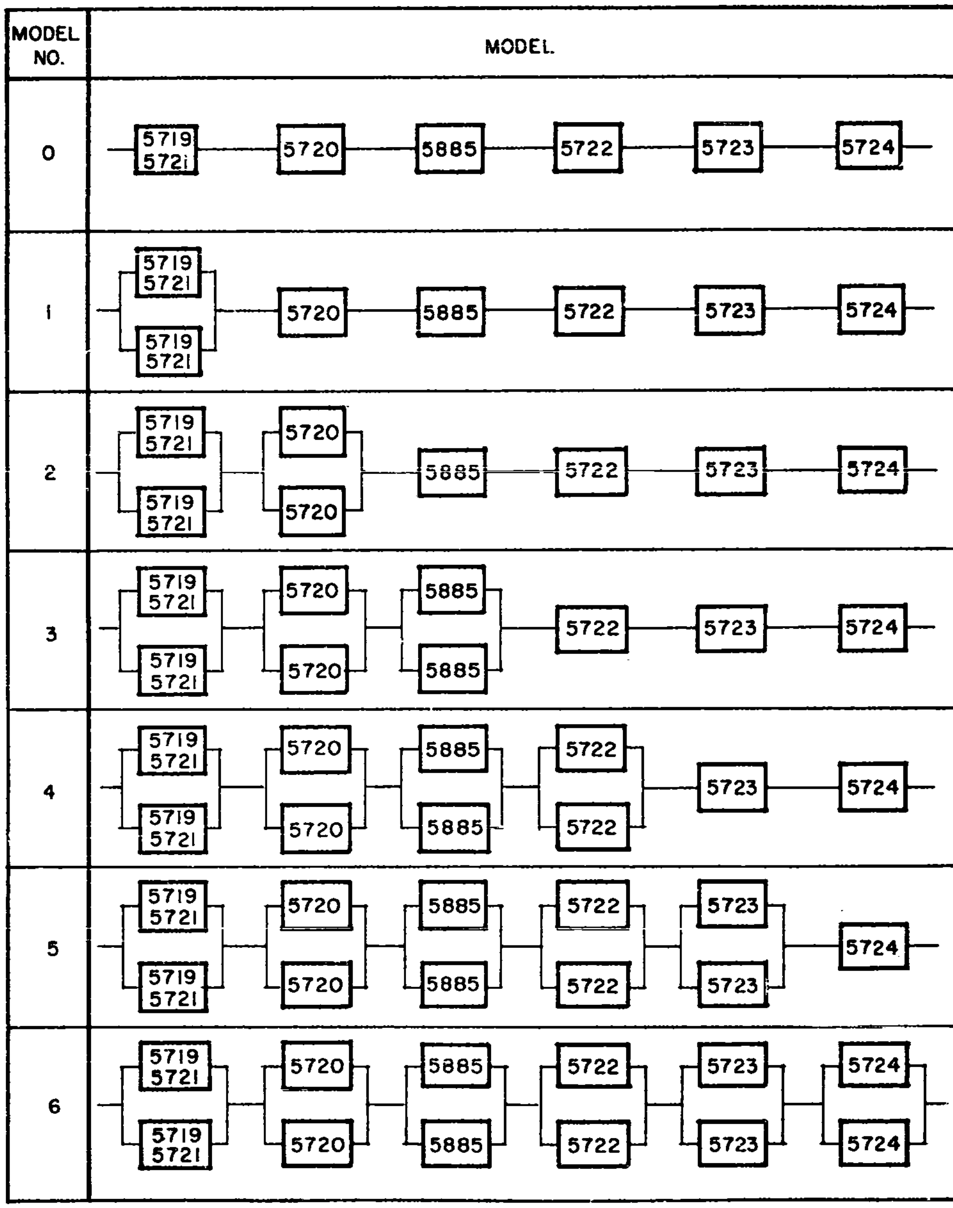


Figure 8-9. Models used for hydraulic/pneumatic test set

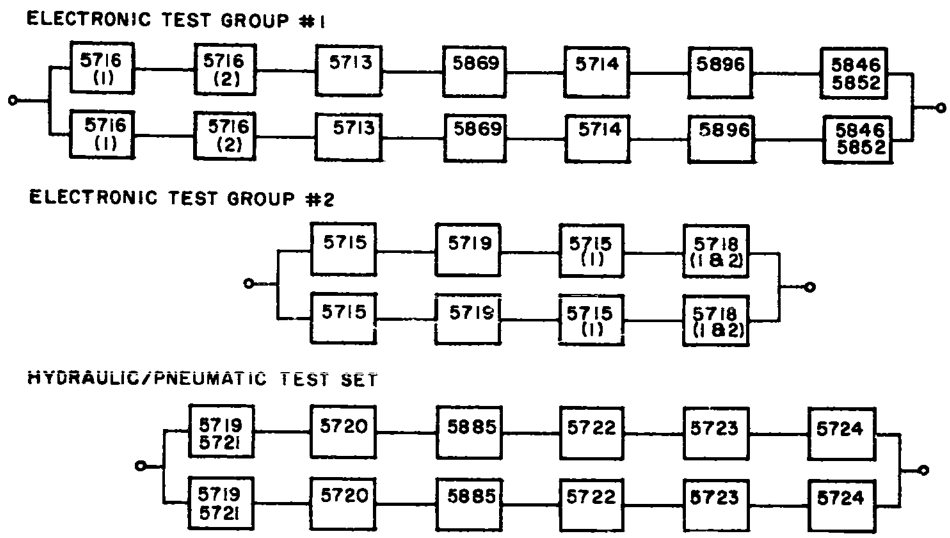


Figure 8-10. System redundancy models

Table 8-6. Failure rate (F. R.) summary at 25°C

Minimodule	Number	F. R. %/1000 hrs. Per Circuit	No. of Circuit Per Millimodule	Total F. R. %/ 1000 hrs. Per Minimodule	MTBF (Hrs.) Per Minimodule
1 Mc Flip Flop	1733458 501	.136	1	.136	735,000
10 Mc Flip Flop	1733451-503	.134	1	.134	746,000
1 Mc Gate	1733459-501	.068	2	.136	735,000
10 Mc Gate	1733459-503	.067	2	.134	746,000
Power Amplifier/ Line Driver	1733460-501	.067	2	.134	746,000
1 Mc Trigger	1733461-501	.013	4	.052	1,923,000
10 Mc Trigger	1733461-503	.023	4	.092	1,087,000
Diode Cluster	1733462-501	.020	4	.080	1,250,000
Relay/Lamp Driver	1733463-501	.111	1	.111	909,000
Power Inverter/ Line Driver	1733843-	.069	2	.138	725,000
Exclusive NOR	1733847-	.168	1	.168	595,000

Table 8-7. Failure rate (F. R.) summary at [illegible]°C

Minimodule	Number	F. R. %/1000 hrs. Per Circuit	No. of Circuit Per Millimodule	Total F. R. %/ 1000 hrs. Per Minimodule	MTBF (Hrs.) Per Minimodule
1 Mc Flip Flop	1733459-501	.142	1	.142	704,000
10 Mc Flip Flop	1733458-503	.140	1	.140	714,000
1 Mc Gate	1733459-501	.071	2	.142	704,000
10 Mc Gate	1733459-503	.070	2	.140	714,000
Power Amplifier/ Line Driver	1733460-501	.072	2	.144	694,000
1 Mc Trigger	1733461-501	.014	4	.056	1,785,000
10 Mc Trigger	1733461-503	.024	4	.096	1,042,000
Diode Cluster	1733462-501	.020	4	.080	1,250,000
Relay/Lamp Driver	1733463-501	.146	1	.146	685,000
Power Inverter/ Line Driver	1733843-	.074	2	.148	676,000
Exclusive NOR	1733842-	.175	1	.175	571,000

The results are shown in Figure 8-11*. The coefficient of variation ($\sigma / \bar{X}$) was plotted against sample size for various levels of accuracy at 90% confidence.

Since the coefficient of variation for maintenance time is not known for MTE, a value of 0. 284 based on observed field data* can be used until specific information on MTE is available. By referring to the curves of Figure 8-11* it can be seen that a sample size of 50 will permit stating the mean maintenance down time with an accuracy of between ±5 and 10% with a confidence of 90% using the value of 0. 284 for the coefficient of variation. As maintenance data becomes available, an actual value for the coefficient of variation can be determined. If it is higher than 0. 284, the sample size may have to be increased to obtain the desired prediction accuracy. If lower, the reverse would of course be true.

C. Task Selection

In order to select the actual maintenance tasks to be evaluated, it is first necessary to apportion the 50 tasks among the various racks of equipment according to the particular rack contribution to the total failure rate of the system. Using predicted failure rate data generated by the reliability group, the number of tasks for each rack was determined. Table 8-8 lists the various equipments of the MTE system, the per cent contribution to the total failure for each rack, and the number of tasks that will be selected from each rack for evaluation.

* RADC TDR-62-156 Maintainability Prediction Technique (Phase IV Progress Report) Dated 15 March 1962.

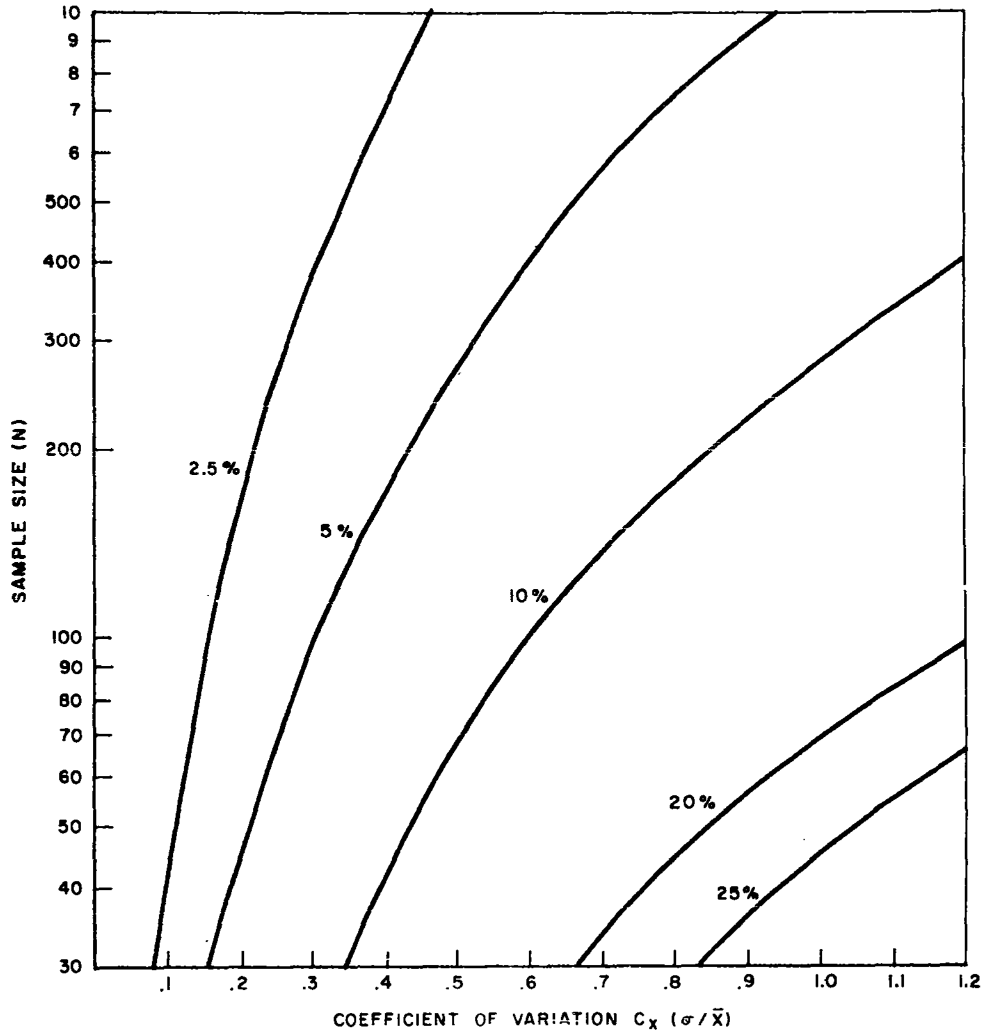


Figure 8-11. Sample size nomograph

Table 8-8. Failure rate contributions

Equipment	Percent Contribution To Total Failure Rate	Sample Size
Computer Controller	15.7	8
Operator Control Console	11.1	5
Measurements	5.2	3
Hi-Frequency Stimulus (Rack 1)	28.7	14
Hi-Frequency Stimulus (Rack 2)	15.8	8
Tape Transport	1.8	1
Low Frequency Stimulus (Rack 1)	4.4	2
Low Frequency Stimulus (Rack 2)	9.6	5
DC Stimuli	7.2	4
DC Int. Power (Rack 1)	0.2	0
DC Int. Power (Rack 2)	0.3	0
TOTAL	100.0	50

Figure 8-12 shows graphically the percent of the total failure rate for the Electronics Test Group that each category of equipment contributes. The percentages shown here are the same as those of Table 8-8 except for equipment grouping. For example, the two racks of equipment making up the High Frequency Unit are lumped together in Figure 8-12. Referring to this Figure, it can be seen that the High Frequency Stimulus Units will be the greatest contributors to maintenance down time. Based on the present preliminary reliability predictions, these two racks account for 44.5% of the total failure rate for the Electronics Test Group. For this reason twenty two of the selected maintenance tasks will be taken from the High Frequency Stimulus Units.

D. Preliminary Prediction - High Frequency Stimulus Units

A review of the preliminary parts list for the High Frequency Stimulus Units reveals that there are approximately twenty-five waveguide switches in the X-band portion of the system. These switches are the heaviest contributors to the failure rate of the high frequency equipment, and it follows that waveguide switch failure will be the most likely mode of failure for these units. In view

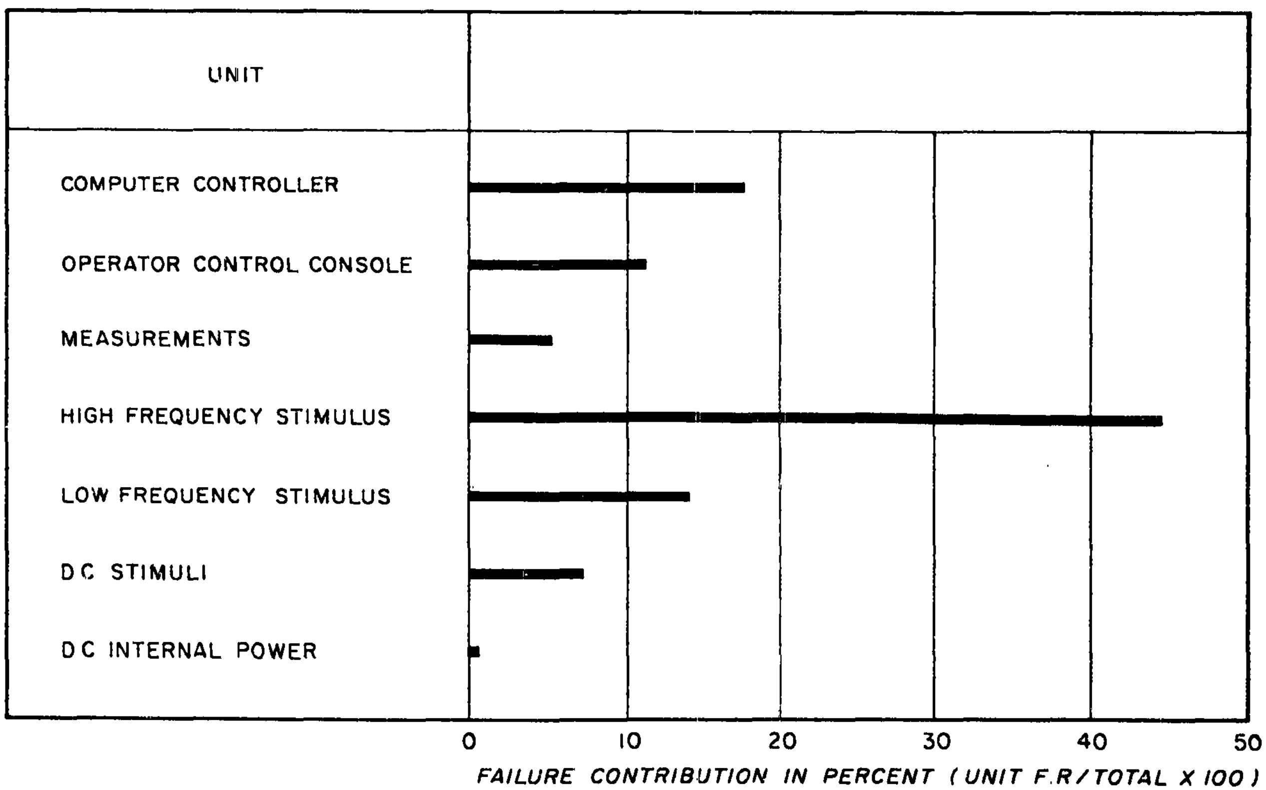


Figure 8-12. MTE failure contribution profile

of the above observations, the mean down time resulting from waveguide switch failures will in all likelihood be very representative of the overall mean down time for the High Frequency Units On the basis of a 50-task sample size, this figure will also weigh very heavily in the determination of the mean down time for the entire system.

E. X Band Input/Output

A preliminary evaluation has been made on the X Band Input/Output drawer, specification No. 5843 of the High Frequency Stimulus Unit. This drawer is typical of three others which contain the waveguide switches;

No. 5845 - X Band Converter
No. 5844 - X Band
No. 5847 - X Band Extender

Table 8-9 shows the results of scoring Checklist A which considers the various physical design factors of an equipment. (See Report No. CR-62-574-9 Product Assurance Program Plan dated 6 July 1962.) The intent of this checklist is to determine the impact of equipment packaging, physical layout, etc., upon maintenance time. In scoring the Input/Output drawer a waveguide switch failure was assumed, and the scoring reflects the conditions and events that would occur in locating and repairing this failure and checking out the equipment once the repair had been made. From Table 8-9 it can be seen that a total score of 43 was obtained as a result of this preliminary evaluation.

To obtain a preliminary down time estimate an average score was assumed for the remaining two checklists, B and C. Checklist B evaluates the need for external facilities such as test equipment, connectors, and technical assistance from other maintenance personnel.

Checklist C evaluates the personnel requirement relating to physical, mental and attitude characteristics, as imposed by the maintenance task. An average score for checklist B is 14 points and for checklist C, 20 points. Applying these values to the equation for maintenance down time, the value of 66 minutes is obtained, as shown below.

8.1.2 MAINTAINABILITY

A. Maintainability Prediction

During this reporting period work was started on the maintainability prediction for MTE. This prediction will utilize the checklist correlation techniques developed by RCA and as described in detail in the MTE Product Assurance Program Plan Report No. CR-62-547-9, dated 6 July 1962.

Due to the complexity of the MTE system, it would not be practical to evaluate the contribution of each replaceable part or component to maintenance time. However, since the physical arrangement and function of many of these components are similar with respect to the maintenance task, it is only necessary to select components which will, on the average, be representative of maintenance tasks which can be expected to occur under operational conditions. Such a sample from an equipment will permit its maintainability to be accurately predicted.

B. Sample Size

The sample size to be used in the prediction is dependent upon the statistical accuracy desired. With stated accuracy requirements (k) and desired confidence interval, the sample size (N) which satisfies these requirements is computed as follows:

$$N = \left(\frac{\phi \sigma}{k \bar{X}} \right)^2$$

Where:

ϕ = Confidence Level
σ = Population Variance
$\bar{X}$ = Population Mean
k = Accuracy

This equation has been solved for a number of values.

$$\log M_{c_t} = 3.54651 - 0.02512A - 0.03055B - 0.01093C \text{ *}$$

Where:

M_{c_t} = Down Time in Minutes

$A = 43$ (Checklist A Score)

$B = 14$ (Checklist B Score)

$C = 20$ (Checklist C Score)

$$\log M_{c_t} = 1.82005$$

$$M_{c_t} = 66 \text{ minutes}$$

The 66-minute figure obtained above represents, as stated previously, a preliminary figure based on one particular task which will be one of the most significant contributors to maintenance down time for the High Frequency Stimulus portion of the MTE system. It is based on average scores for the facilities and human factors considerations, since sufficient information does not exist at this time to properly score Checklists B and C.

8.1.3 SAFETY

The latest equipment configurations have been reviewed for potential safety problems. In reviewing the design, both electrical and mechanical aspects are considered. In the area of electrical design, the following items are among those considered:

(1) Grounding Practices
(2) Adequate Safety Covers
(3) Interlock Switches
(4) Discharging Devices
(5) Circuit Protection Devices

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* RADC TDR-62-156 Maintainability Prediction Techniques (Phase IV Progress Report) Dated 15 March 1962

In the mechanical area the equipment design is checked to insure that suitable protection has been provided to prevent personnel contact with moving mechanical parts such as gears, fans and belts. Stops should be provided on chassis slides to prevent pulling the chassis too far out and dropping it. Suitable handles or similar provisions should be furnished for removing from enclosures.

As the program moves into the fabrication phase, the equipment will be reviewed on a continuing basis to insure that any potential safety problems overlooked during the design phase, are corrected prior to delivery to the customer. This effort will continue during the test phase.

8.1.4 VALUE ENGINEERING

(1) Addenda to the Value Engineering Value Manual are being developed. The subject of one is, "The Preparation and Use of the Functional Chart".
(2) Initial orientation of program management in Value Engineering has started. To date, fifteen people have been oriented or trained with additional programs scheduled for April.
(3) Subcontractor orientation and training plans have been undertaken. Both programs are to be completed in the 5th quarter.
(4) Study efforts are continuing on high and/or unnecessary cost areas of the system.

8.2 PLANS

8.2.1 RELIABILITY

(1) The reliability stress analysis effort will continue on all units.
(2) Based on the stress analysis, reliability will identify units that are not meeting their apportioned goal and will present recommendations for improvement.
(3) Design levels for the laboratory test program will be established.
(4) Reliability will commence writing test plans.
(5) Participation in design reviews will continue.

8.2.2 MAINTAINABILITY

The major effort in the maintainability area during the next reporting period will be devoted to the maintainability prediction. As detailed design information becomes available on the various units, detailed maintainability analysis will be performed on selected tasks to determine quantative maintainability indices for the MTE system.

8.2.3 SAFETY

(1) Review of the latest equipment design data will continue as changes are made and the system configuration is finalized.
(2) Safety design guidelines will be updated as required.
(3) A review of hydraulic equipment design information will begin to insure that adequate safety provisions have been incorporated.

8.2.4 VALUE ENGINEERING

(1) Complete the addendum to the Value Engineering Manual.
(2) Continue value orientation and task group seminar for better design cost analysis.
(3) Continue training and monitoring of subcontractor value engineering programs.
(4) Continue evaluation of value engineering upon program design and procurement.

APPENDIX A

PRELIMINARY PURCHASE SPECIFICATIONS

ENVIRONMENTAL AND SERVICE CONDITIONS
MULTISYSTEM TEST EQUIPMENT

APPENDIX A

PRELIMINARY PURCHASE DESCRIPTION

ENVIRONMENTAL AND SERVICE CONDITIONS
MULTISYSTEM TEST EQUIPMENT

1. SCOPE

1.1 Scope. - This specification covers the environmental and service conditions requirements for four types of construction for the Multisystem Test Equipment (MTE).

1.2 Classification. - The four types of MTE construction are as follows:

Type I — Shelter

Type II — Rack, Electrical Assembly

Type III — Chassis, Electrical Assembly

Type IV — Console, Hydraulic Assembly

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification insofar as they form sources of reference data.

SPECIFICATIONS

Military

MIL-E-4970A	General Specifications for Ground Support Equipment Environmental Testing

STANDARDS

Military

MIL-STD-210A	Climatic Extremes for Military Equipment
MIL-STD-446	Environmental Requirements for Electronic Component Parts

PUBLICATIONS

Army

AR 705-8	Department of Defense Engineering for Transportability Program
AR 705-15	Operation of Material under Extreme Conditions of Environment
AR 705-35	Criteria for Air-Transportability and Delivery of Materials
AR 715-56 (M205)	Military Outline of Form and Instructions for the Preparation of Specifications

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specified procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Shelter.

3.1.1 Vibration. - The shelter shall not be damaged nor shall its performance be impaired when subjected to the following conditions:

a. 3 g's from 2-1/2 cps to 50 cps

b. 10 g's from 50 cps to 70 cps

c. 5 g's from 70 cps to 500 cps

3.1.2 Shock. - The shelter shall not be damaged nor shall its performance be impaired when subjected to the following conditions:

a. $\pm$20 g in the vertical plane

b. $\pm$20 g in the horizontal plane

c. $\pm$10 g in the transverse plane

3.1.3 Temperatures. - The shelter shall not be damaged nor shall its performance be impaired when subjected to varying temperatures ranging from minus 53.9°C to 71.1°C (minus 65°F to 160°F) including maximum solar radiation of 360 British thermal units (Btu) per square foot.

3.1.4 Wind.

3.1.4.1 Limited operation. — The shelter shall not be damaged nor shall its performance be impaired when subjected to steady winds of 60 miles per hour (mph) with gusts of 90 mph.

3.1.4.2 Nonoperational with tie downs. - The shelter shall not be damaged nor shall its performance be impaired when subjected to steady winds of 80 mph with gusts of 120 mph.

3.1.5 Snow. - The shelter shall not be damaged nor shall its performance be impaired when subjected to a snow accumulation load, over a 150-day period, amounting to 40 pounds per square foot.

3.1.6 Rain. - The shelter shall not be damaged nor shall its performance be impaired when subjected to an accumulation of 12 inches in 11 hours 55 minutes with as much as 7 inches in one hour and 2 inches in 5 minutes, nor shall there be leakage when it is immersed in 21 inches of salt water for 30 minutes.

3.1.7 Relative humidity. - The shelter shall not be damaged nor shall its performance be impaired when subjected to relative humidities up to and including 100 percent.

3.1.8 Ambient pressure. - The shelter shall not be damaged nor its performance be impaired when subjected to varying pressures from 31.3 inches of mercury (in. Hg) to 3.4 in. Hg.

3.1.9 Salt-laden air. - The shelter shall not be damaged nor shall its performance be impaired when subjected to salt-laden air as encountered in coastal regions or during ocean transport.

3.1.10 Fungus. - The shelter shall not be damaged nor shall its performance be impaired when subjected to fungus growth as encountered in tropical climates.

3.1.11 Sand and dust. - The shelter shall not be damaged nor shall its performance be impaired when subjected to sand and dust as encountered in desert areas.

3.2 Rack.

3.2.1 Vibration. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to the following conditions:

a. 4.5 g's from 2-1/2 to 30 cps
b. 2 g's from 30 cps to 500 cps

3.2.2 Shock. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to three shocks. Each shock shall approximate a half-sinusoid, have a total duration of 30 $\pm$1 milliseconds along each of the three principal axes, and have the following magnitudes (9 shocks):

$\pm$10 g in all directions

3.2.3 Temperature.

3.2.3.1 Storage and transportation. - The full assembled rack shall operate satisfactorily after having been subjected to an ambient temperature range of minus 53.9°C to 71.1°C (minus 65°F to 160°F).

3.2.3.2 Operable within tolerance. - The fully assembled rack shall have no degradation of its performance when subjected to varying temperatures ranging from minus 18°C to 51.7°C (0°F to 125°F).

3.2.4 Relative Humidity. - The full assembled rack shall not be damaged nor shall its performance be impaired when subjected to relative humidities up to and including 100 percent with heavy condensation at startup.

3.2.5 Ambient pressure. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to the following ranges of pressure:

a. Operational - 31.3 in. Hg to 20.6 in. Hg.

b. Non-operational (storage) - 31.3 in. Hg to 3.4 in. Hg.

3.2.6 Salt-laden air. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to salt-laden air as encountered in coastal regions.

3.2.7 Fungus. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to fungus growth as encountered in tropical climates.

3.2.8 Sand and dust. - The fully assembled rack shall not be damaged nor shall its performance be impaired when subjected to sand and dust as encountered in desert areas.

3.3 Chassis.

3.3.1 Vibration. - The fully assembled chassis shall not be damaged nor shall its performance be impaired when subjected to the following conditions:

3.3.8 Sand and dust. – The fully assembled chassis shall not be damaged nor shall its performance be impaired when subjected to sand and dust as encountered in desert areas.

3.4 Console.

3.4.1 Vibration. – The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to the following conditions:

a. 4.5 g from 2-1/2 cps to 30 cps

b. 2 g from 30 cps to 500 cps

3.4.2 Shock. – The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to three shocks. Each shock shall approximate a half-sinusoid, have a total duration of 30 $\pm$1 milliseconds along each of the three principal axes, and have the following magnitudes (9 shocks):

$\pm$10 g in all directions

3.4.3 Temperature.

3.4.3.1 Storage and transportation. – The fully assembled console shall operate satisfactorily after having been subjected to an ambient temperature range of minus 53.9°C to 71.1°C (minus 65°F to 160°F).

3.4.3.2 Operable within tolerance. – The fully assembled console shall have no degradation of its performance when subjected to varying temperatures ranging from minus 18°C to 51.7°C (0°F to 125°F).

3.4.4 Relative humidity. – The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to relative humidities up to and including 100 percent with heavy condensation at startup.

3.4.5 Ambient pressure. – The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to the following ranges of pressure

a. Operational – 31.3 in. Hg to 20.6 in. Hg.

b. Non-operational (storage) – 31.3 in. Hg to 3.4 in. Hg.

3.4.6 Salt-laden air. - The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to salt-laden air as encountered in coastal regions.

3.4.7 Fungus. - The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to fungus growth as encountered in tropical climates.

3.4.8 Sand and dust. - The fully assembled console shall not be damaged nor shall its performance be impaired when subjected to sand and dust as encountered in desert areas.

4. QUALITY ASSURANCE PROVISIONS

4.1 General quality assurance provisions.

4.1.1 Contractor inspection. - Unless otherwise specified herein, the supplier is responsible for the performance of all inspection requirements prior to submission for Government inspection and acceptance. Except as otherwise specified, the supplier may utilize his own facilities or any commercial laboratory acceptable to the Government. Inspection records of the examination and tests shall be kept complete and available to the Government as specified in the contract or order.

4.1.2 Examination.

4.1.2.1 Visual examination. - The unit under test shall be examined visually for damage and to determine compliance with its detail specifications or drawings at the beginning and at the conclusion of each test, or phase of a test, during which the unit may have sustained damage.

4.1.2.2 Inspection testing. - The unit shall be functionally tested to determine compliance with its detail specifications or drawings prior to each environmental test to which the unit is to be subjected. Unless otherwise specified, the unit shall again be functionally tested to determine compliance with its detail specifications or drawings at the conclusion of each test, or phase of a test, during which failure may have occurred, after the equipment has been stabilized to standard conditions.

4.1.2.3 Testing tolerances. - The maximum allowable tolerances for test conditions (see 4.1.2.4) shall be as follows (exclusive of accuracy of instruments):

a. Temperature: $\pm 2.2^{\circ}C$ ($4^{\circ}F$)
b. Altitude: ± 5 percent
c. Relative humidity: +5, -0 percent
d. Force amplitude: ± 10 percent
e. Force frequency: ± 2 percent
f. Additional tolerances: Additional tolerances shall be as specified herein

4.1.2.4 Standard test conditions. - Conditions for conducting tests shall be as follows, unless otherwise specified in detail specifications:

a.	Temperature:	$25^{o}C \pm 10^{o}C$ ($77^{o}F \pm 18^{o}F$)
b.	Altitude:	0 to 4500 feet (0 to 1500 meters) above sea level.
c.	Humidity:	90 percent or less (relative)
d.	Barometric Pressure:	28 to 32 inches (71.12 to 71.28 centimeters) of mercury

4.1.2.5 Environmental testing. - Environmental testing to determine compliance of the unit with the service condition requirements specified herein shall be conducted in accordance with the corresponding test paragraphs indicated in Table I. Unless otherwise specified all test equipment shall be non-operational during environmental testing.

4.2 Environmental tests.

4.2.1 Vibration.

4.2.1.1 Unit. - Drive the properly mounted unit at standard test conditions over the Munson and cross-country courses for track and wheeled vehicles at Aberdeen Proving Ground; then test for satisfactory performance.

4.2.1.2 Rack. - The vibration test shall be conducted by mounting the rack rigidly on suitable vibration test apparatus in a position dynamically similar to the most severe position likely to be encountered in service.

4.2.1.2.1 Resonance. - Resonant frequencies of the rack shall be determined by varying the frequencies of applied vibration slowly through the 2 to f_n cps range of frequencies at vibratory conditions not to exceed those of 3.2.1 of this specification. The search procedure shall be followed successively with vibrations applied along three mutually perpendicular axes of the rack. The rack shall be vibrated at each indicated resonant condition for 3 hours. When more than one resonant frequency is encountered with vibration applied along any one axis, the test period may be accomplished at the most severe resonance, or the period may be divided among the resonant frequencies, whichever is considered most likely

Table I. Correlation of environmental testing and requirements

	Service Condition Requirements				Environmental Test			
	Shelter (ref)	Rack (ref)	Chassis (ref)	Console (ref)	Shelter or Unit[1] (ref)	Rack (ref)	Chassis (ref)	Console (ref)
Vibration	3.1.1	3.2.1	3.3.1	3.4.1	4.2.1.1	4.2.1.2	4.2.1.3	4.2.1.4
Shock	3.1.2	3.2.2	3.3.2	3.4.2	4.2.2.1	4.2.2.2	4.2.2.3	4.2.2.4
Temperature	3.1.3	3.2.3	3.3.3	3.4.3	4.2.3.1	4.2.3.2	4.2.3.3	4.2.3.4
Wind	3.1.4	NA[2]	NA	NA	4.2.4	NA	NA	NA
Snow	3.1.5	NA	NA	NA	4.2.5	NA	NA	NA
Rain	3.1.6	NA	NA	NA	4.2.6	NA	NA	NA
Relative Humidity	3.1.7	3.2.4	3.3.4	3.4.4	4.2.7.1	4.2.7.2	4.2.7.3	4.2.7.4
Ambient Pressure	3.1.8	3.2.5	3.3.5	3.4.5	4.2.8.1	4.2.8.2	4.2.8.3	4.2.8.4
Salt-Laden Air	3.1.9	3.2.6	3.3.6	3.4.6	4.2.9.1	4.2.9.2	4.2.9.3	4.2.9.4
Fungus	3.1.10	3.2.7	3.3.7	3.4.7	4.2.10.1	4.2.10.2	4.2.10.3	4.2.10.4
Sand and Dust	3.1.11	3.2.8	3.3.8	3.4.8	4.2.11.1	4.2.11.2	4.2.11.3	4.2.11.4

[1] As specified (See 6.3).

[2] NA = not applicable

to produce failure. When resonant conditions are not apparent within the specified frequency range, the rack shall be vibrated under the cycling conditions specified in 4. 2. 1. 2. 2 below for a period of 4 hours instead of the 1 hour specified therein.

4. 2. 1. 2. 2 Cycling. - Cycling vibration shall be applied along each of 3 mutually perpendicular axes for 1 hour. The test shall be conducted with the vibration frequency varying at the logarithmic rate of change of 1/2 octave per minute between the limits of 30 and f_n cps. The acceleration applied shall be plus or minus 2. 0 g.

4. 2. 1. 3 Chassis. - The chassis shall be subjected to vibration tests in accordance with 4. 2. 1. 2 of this specification.

4. 2. 1. 4 Console. - The console shall be subjected to vibration test in ac~~cordance with 4. 2. 1. 2 of this specification.~~

4. 2. 2 Shock.

4. 2. 2. 1 Unit. - The unit shall be subjected to tests to determine effects of shock, both for items with shock isolators and others.

4. 2. 2. 1. 1 Edgewise-drop tests. - One edge of the unit shall be rigidly supported 4 inches above a hard, level concrete surface. The opposite end shall be raised and allowed to fall freely from a height of 12 inches This test shall be applied once to each end of the shelter.

4. 2. 2. 1. 2 Cornerwise-drop tests. - One corner of the base of the unit shall be supported on a block approximately 5 inches in height. A block nominally 12 inches in height shall be placed under the other corner of the same end. The opposite end of the shelter shall be raised and allowed to fall freely to a hard, level concrete surface from a height of 12 inches. This test shall be applied once to each of two diagonally opposite corners of the base.

4. 2. 2. 1. 3 Face-drop tests. - The unit shall be dropped on its base onto a hard, level concrete surface, falling freely through the vertical distance of 12 inches. Prior to each drop, the unit shall be suspended with the base parallel to the impact surface.

4.2.2.1.4 Operational tests. - Drive the properly mounted unit at standard test conditions over the Munson and cross-country courses for track and wheeled vehicles at Aberdeen Proving Grounds; then test for satisfactory performance. (This test is a duplication of that in 4.2.1 and shall be run simultaneously.)

4.2.2.2 Rack. - The rack shall be secured to the test plate of a shock testing machine in the position that the equipment will occupy in use. Any shock isolator used in the equipment shall be in place and unblocked. Three shocks shall be applied along each of three mutually perpendicular directions that are respectively parallel to the edges of the equipment (a total of 9 shocks). The three shocks applied along each direction shall each be sufficient to result in a 10-g shock of 30 milliseconds. The equipment shall not be energized during the test. Performance shall be measured at the conclusion of the test period along each direction.

4.2.2.3 Chassis. - The chassis shall be subjected to shock tests in accordance with 4.2.2.2 of this specification.

4.2.2.4 Console. - The console shall be subjected to shock tests in accordance with 4.2.2.2 of this specification.

4.2.3 Temperature. - The equipment shall be subjected to extreme temperature tests to determine the resistance of the equipment to temperatures that may be encountered during the service life of the equipment either in storage or under operational conditions.

4.2.3.1 Shelter.

4.2.3.1.1 High-temperature tests. - The shelter shall be placed within a high-temperature chamber, and the internal temperature of the chamber shall be raised to 71°C (160°F) with an internal relative humidity of not more than 15 percent. The shelter shall be maintained at these conditions for a period of 48 hours. At the end of the test period, while at testing conditions, the shelter shall be examined visually and functionally tested.

4.2.3.1.2 Radiation (sunshine). - The shelter shall be subjected to tests to determine the effect of radiant energy on the equipment.

4.2.3.1.2.1 Procedure. - The shelter shall be placed within a test chamber and exposed to radiant energy at the rate of 100 to 140 watts per square foot. Fifty to 84 watts per square foot of the total energy shall be in wavelengths above 7800 angstrom units and 4 to 8 watts per square foot in wavelengths below 3800 angstrom units. The test chamber shall be maintained at 45°C (113°F) during the course of the test which shall not be less than 48 hours. At the conclusion of the test period, while at testing conditions, the shelter shall be visually inspected for flaking and chipping of painted surfaces, and checking and crazing of natural rubber and plastics.

4.2.3.1.3 Low-temperature tests. - The shelter shall be placed within a cold-temperature chamber and the internal temperature of the chamber shall be lowered to minus 53.9°C (minus 65°F) and maintained at this temperature for a period of 48 hours. Visually inspect and functionally test the shelter, at the test conditions, at the conclusion of the test period.

4.2.3.2 Rack.

4.2.3.2.1 High-temperature tests (storage and operation). - The rack shall be placed within a high-temperature chamber. The internal temperature shall be raised to 71.1°C (160°F) with an internal relative humidity of not more than 15 percent. The rack shall be maintained at these conditions for 48 hours. At the conclusion of the test period, while at testing conditions, visually inspect the equipment. The temperature of the chamber shall then be lowered to 51.9°C (125°F) and maintained at these conditions for 4 hours. At the end of the test period, while at testing conditions, visually inspect the equipment and operate in accordance with 3.2.3.2 of this specification.

4.2.3.2.2 Low-temperature tests (storage and operation). - The rack shall be placed within a cold-temperature chamber and the internal temperature of the chamber shall be lowered to minus 53.9°C (minus 65°F) and maintained at this temperature for a period of 48 hours. At the end of the test period, while at this

temperature, visually inspect. The temperature of the chamber shall then be raised to minus 18°C (0°F) and maintained for an additional 4 hours. At the conclusion of this exposure period and while at this temperature, the equipment shall be functionally tested and visually inspected.

4.2.3.3 Chassis.

4.2.3.3.1 High-temperature tests (storage and operation). - The chassis shall be tested in accordance with the procedures detailed in 4.2.3.2.1 of this specification.

4.2.3.3.2 Low-temperature tests (storage and operation). - The chassis shall be tested in accordance with the procedures detailed in 4.2.3.2.2 of this specification.

4.2.3.4 Console.

4.2.3.4.1 High-temperature tests (storage and operation). - The console shall be tested in accordance with the procedures detailed in 4.2.3.2.1 of this specification.

4.2.3.4.2 Low-temperature tests (storage and operation). - The console shall be tested in accordance with the procedures detailed in 4.2.3.2.2 of this specification.

4.2.4 Wind. - The unit shall be qualified to determine its resistance to winds to be encountered as specified in Specification MTE-070.

4.2.5 Snow. - The roof of the shelter shall be qualified as specified in Specification MTE-070.

4.2.6 Rain. - The shelter shall be subjected to rain tests to determine the ability of protecting the equipment. Therefore it shall be placed in its normal operating position, in a test chamber maintained at 21.1°C ±2.8°C (70°F ±5°F). Allow simulated rain water to fall freely and directly on the shelter at a rate as prescribed in Table II for a 24-hour cycle. The entire shelter shall be exposed to the uniformly dispersed rainfall. At the conclusion of the test examine the shelter, including external electrical receptacles, for evidence of water penetration,

free water, swelling, or other penetration. The shelter shall then be immersed in 21 inches of salt water for 30 minutes; leakage shall be cause for rejection.

Table II. Precipitation

Amount (in.)	12	2	11	7
Duration (hr:min)	11:55	0:05	11:00	1:00
Drop Size Mean (mm)	2:25	4.0	2.25	3.2
Standard Deviation	0.77	1.68	0.77	1.1
Wind Speed (mph)	0	0	40	0

4.2.7 Relative humidity.

4.2.7.1 Shelter. - The shelter shall be subjected to humidity tests to determine the resistance of the shelter to the effects of exposure to a warm highly humid atmosphere such as is found in tropical areas.

4.2.7.1.1 Procedure. - The shelter shall be placed in a test chamber and set up to simulate installed conditions. The test chamber shall be vented to the atmosphere to prevent the buildup of pressure. During the first 2-hour period, the temperature within the chamber shall be gradually raised to 71°C (160°F) and maintained at this temperature for 6 hours. The velocity of the air throughout the test area shall not exceed 150 feet per minute. During the following 16-hour period, the temperature in the chamber shall be gradually reduced to 24°C (75°F), which constitutes one cycle. The relative humidity throughout the cycle shall be at least 95 percent. The cycle shall be repeated for a total test time of 240 hours (10 continuous cycles). At the conclusion of the 240-hour period, the equipment shall be returned to standard conditions, and the moisture removed by wiping, but without disassembly or by application of heat from an external source. Drying by air blast will not be permitted. As soon as possible after completion of the test period, the shelter shall be visually inspected and functionally tested.

4.2.7.2 Rack. - The rack shall be subjected to the humidity test in accordance with 4.2.7.1 of this specification.

4.2.7.3 Chassis. - The chassis shall be subjected to the humidity test in accordance with 4.2.7.1 of this specification.

4.2.7.4 Console. - The console shall be subjected to the humidity test in accordance with 4.2.7.1 of this specification.

4.2.8 Ambient pressure.

4.2.8.1 Shelter. - The shelter shall be subjected to extreme pressurization tests to determine the ability of the shelter to operate satisfactorily under these conditions. Therefore it shall be placed within an altitude pressurization chamber. The internal absolute pressure shall be reduced to 3.42 in. of Hg (corresponding to an altitude of 50,000 feet above sea level with an ambient temperature at 25°C (77°F)). The duration of the test period shall be 1 hour. At the conclusion of this period, the pressure shall be raised to that of local ground conditions and the shelter inspected visually and functionally tested.

4.2.8.2 Rack.

4.2.8.2.1 Operational. - The rack shall be tested in accordance with 4.2.8.1 of this specification except that the altitude levels and their related absolute pressures specified in 3.2.6 of this specification shall be used.

4.2.8.2.2 Non-operational. - The rack shall be tested in accordance with 4.2.8.1 of this specification.

4.2.8.3 Chassis

4.2.8.3.1 Operational. - The chassis shall be tested in accordance with 4.2.8.1 of this specification except that the altitude levels and their related absolute pressures specified in 3.3.5 of this specification shall be used.

4.2.8.3.2 Non-operational. - The chassis shall be tested in accordance with 4.2.8.1 of this specification.

4.2.8.4 Console.

4.2.8.4.1 Operational. - The console shall be tested in accordance with 4.2.8.1 of this specification except that the altitude levels and their

related absolute pressures specified in 3.4.5 of this specification shall be used.

4.2.8.4.1 Non-operational. - The console shall be tested in accordance with 4.2.8.1 of this specification.

4.2.9 Salt-laden air.

4.2.9.1 Shelter. - The shelter shall be subjected to salt-laden air tests for not less than 48 hours to determine its resistance to the effect of a salt atmosphere.

4.2.9.1.1 Apparatus. - The apparatus used in the salt-laden air test shall include the following:

a. Exposure chamber with racks for supporting specimens:

b. Salt solution reservoir

c. Means for atomizing salt solution, including suitable nozzle and compressed air supply

d. Chamber-heating means and control

e. Means for humidifying the air at a temperature above the chamber temperature.

4.2.9.1.2 Chamber. - The chamber and all accessories shall be made of material which will not affect the corrosiveness of the air, such as glass, hard rubber, plastic, or wood other than plywood. In addition, all parts which come in contact with test items shall be of materials that will not cause electrolytic corrosion. The chamber and accessories shall be so constructed and arranged that there is not direct impingement of the spray or dripping of the condensate on the test items, that the air circulates freely about all items to the same degree, and that no liquid which has come in contact with the test specimens returns to the salt-solution reservoir. The chamber shall be properly vented and be capable of being regulated to and maintained at 35°C (95°F) for the duration of the test.

4.2.9.1.3 Atomizer. - The atomizers used shall be of such design and construction as to produce a finely divided, wet, dense fog.

4.2.9.1.4 Air supply. - The compressed air entering the atomizers shall be free from all impurities, such as oil and dirt. Means shall be provided to humidify and warm the compressed air as required to meet the operating conditions. The air pressure shall be suitable to produce a finely divided dense fog with the atomizer used. To ensure against clogging the atomizers by salt deposition, the air should have a relative humidity of at least 85 percent at the point release from the nozzle. A satisfactory method is to pass the air in very fine bubbles through a tower containing heated water. The temperature of the water should be 35°C (95°F) and often higher. The permissible water temperature increases with increasing volume of air and with decreasing heat insulation of the chamber and temperature of the chamber's surroundings. It should not exceed the value above which an excess of moisture is introduced into the chamber (for example, 43°C (109°F) at an air pressure of 12 psi) or a value which makes it impossible to meet the requirement for operating temperature.

4.2.9.1.5 Salt solution. - The salt used shall be sodium chloride containing on the dry basis not more than 0.1 percent of sodium iodide and not more than 0.2 percent of total impurities. The solution shall be prepared by dissolving 20 $\pm$2 parts by weight of salt in 80 parts by weight of distilled or other water containing not more than 200 parts per million of total solids. The solution shall be kept free from solids by filtration or decantation. The solution shall be adjusted to and maintained at a specific gravity of from 1.126 to 1.157 and at a pH value between 6.5 to 7.2 when measured at a temperature between 33° and 36°C (92° and 97°F). Only commercially pure (CP) hydrochloric acid or CP sodium hydroxide shall be used to adjust the pH. The pH measurement shall be made electrometrically using a glass electrode with a saturated potassium chloride bridge or by a colorimetric method such as bromothymol blue, provided the results are equivalent to those obtained with the electrometric method.

4.2.9.2 Rack. - The rack shall be subjected to salt-laden air tests in accordance with 4.2.9.1 of this specification.

4.2.9.3 Chassis. - The chassis shall be subjected to salt-laden air tests in accordance with 4.2.9.1 of this specification.

4.2.9.4 Console. - The console shall be subjected to salt-laden air tests in accordance with 4.2.9.1 of this specification.

4.2.10 Fungus resistance.

4.2.10.1 Shelter. - The fungus resistance test is conducted to determine the resistance of the shelter to fungi.

4.2.10.1.1 Procedure. - Four groups of fungi are listed below, and one species of fungus from each group shall be used. In the preparation of the spore suspension, distilled water having a pH value between 5.8 and 7.2 at temperatures between 22.2°C (72°F) and 31.6°C (89°F) shall be utilized. Approximately 10 milliliters of distilled water shall be introduced directly into a tube culture of the fungus and the spores brought into suspension by gentle rubbing of the spore layer with an inoculating loop without disturbing the agar surface. This process is repeated for each specie of fungi. The separate spore suspensions from the four species of fungi shall be mixed together to provide suspension. Actively sporulating cultures between 7 and 21 days old after initial inoculation shall be used for the preparation of the spore suspension. After preparation the spore suspension will not be kept more than a 24-hour period at temperatures between 22.2°C (72°F) and 31.6°C (89°F) and not more than 48 hours at refrigerator temperatures of 1.6°C to 7.2°C (35°F to 45°F). The shelter, including applicable external connections, shall be placed in a test chamber maintaining an internal temperature of 30°C ±2°C (86°F ±3.6°F) and a relative humidity of 95 percent, and sprayed with the suspension mixed spore. The test period shall be 28 days. At the end of the test period, the shelter shall be examined visually.

4.2.10.1.2 Organisms. - The four groups of fungi are as follows:

Group I Chaetomium globosum 6205 or Myrothecium verracaria 9095

Group II Memenoniella echinata 9597 or Aspergillus niger 6275

Group III Aspergillus flavus 10836 or Aspergilius terreus 10690

Group IV Penicillium citrinum 9849 or Pennicillium ochrochloron 9112

4.2.10.1.3 Stock culture designation and source. - Stock cultures may be obtained from the following source:

American Type Culture Collection
2112 M Street, N.W.
Washington 6, D.C.

4.2.10.2 Rack. - The rack shall be subjected to fungus resistance tests in accordance with 4.2.10.1 of this specification.

4.2.10.3 Chassis. - The chassis shall be subjected to fungus resistance tests in accordance with 4.2.10.1 of this specification.

4.2.10.4 Console. - The console shall be subjected to fungus resistance tests in accordance with 4.2.10.1 of this specification.

4.2.11 Sand and dust.

4.2.11.1 Shelter. - The sand and dust test is conducted to determine the resistance of the shelter to blowing sand and dust particles.

4.2.11.1.1 Procedure. - The shelter shall be placed within a test chamber and the sand and dust density raised to and maintained at 0.1 to 0.25 gram per cubic foot within the test space. The relative humidity shall not exceed 30 percent at any time during the test. Sand and dust used in the test shall be of angular structure and shall have characteristics as follows:

a. 100 percent of the sand and dust shall pass through a 100-mesh screen, U.S. Standard Sieve Series.

b. 98 ±2 percent of the sand and dust shall pass through a 140-mesh screen, U.S. Standard Sieve Series.

c. 90 ±2 percent of the sand and dust shall pass through a 200-mesh screen, U.S. Standard Sieve Series.

d. 75 ±2 percent of the sand and dust shall pass through a 325-mesh screen, U.S. Standard Sieve Series.

e. Chemical analysis of the dust shall be as follows:

Substance	Percent by Weight
SiO_2	97 to 99
Fe_2O_3	0 to 2
Al_2O_3	0 to 1
TiO_2	0 to 2
MgO	0 to 1
Ign Losses	0 to 2

The internal temperature of the test chamber shall be maintained at 25°C (77°F) for a period of 1.5 hours, with sand and dust velocity through the test chamber at 2300 ± 500 feet per minute. After 1.5 hours at the above conditions, the temperature shall be raised to and maintained at 71°C (160°F). At the end of the test period, the shelter shall be removed and allowed to cool to room temperature and shall be functionally tested.

4.2.11.2 Rack. - The rack shall be subjected to sand and dust tests in accordance with 4.2.11.1 of this specification except that the sand and dust velocity through the chamber shall be between 100 and 500 feet per minute.

4.2.11.3 Chassis. - The chassis shall be subjected to sand and dust tests in accordance with 4.2.11.1 of this specification except that the sand and dust velocity through the chamber shall be between 100 and 500 feet per minute.

4.2.11.4 Console. - The console shall be subjected to sand and dust tests in accordance with 4.2.11.1 of this specification except that the sand and dust velocity through the chamber shall be between 100 and 500 feet per minute.

5. PREPARATION FOR DELIVERY

5.1 This section is not applicable.

6. NOTES

6.1 Intended use. - The electrical equipment shelter is intended to house the automatic test and checkout equipment of the MTE. This specification establishes the service condition requirements, and associated environment tests generally applicable to such equipment.

6.2 Ordering data. - Procurement documents should specify:

a. Title, number, and date of this specification.

b. Those tests to which the unit is to be subjected, if complete testing is not to be required.

c. Whether a detail test plan is required, and responsibility for its preparation.

d. Responsibility for conducting tests.

e. Source and quantity of test specimens, and their ultimate disposition.

f. Data to be included in test report, if report is required.

6.3 Vibration and shock tests on the shelter are not required. All tests on the shelter are performed to determine the protection level of internal equipment.

6.4 Definitions. - For the purpose of this specification, the following definitions shall apply:

6.4.1 Unit. - An electrical equipment shelter fully outfitted with its required racks, chassis, and consoles of installed equipment.

6.4.2 Shelter. - An enclosure without wheels (skid-mounted or with handling frame) designed to house electrical or electronic equipment and to accommodate one or more men.

6.4.3 Rack. - The frame designed to house or display electrical or electronic equipment.

6.4.4 Chassis. - The frame designed to accommodate the mounted parts of electrical or electronic equipment.

6.4.5 Console. - The frame designed to accommodate the mounted parts of pneumatic or hydraulic equipment.

6.4.6 Parts - A part is an item which cannot or will not be further disassembled without partial or total destruction of the whole.

6.4.7 Equipment. - A general term meaning any grouping of items.

6.4.8 Procuring agency. - For the purpose of this specification, the procuring agency shall be RCA.

NOTICE: When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

CUSTODIAN:
Army-Ordnance Corps

PREPARING ACTIVITY:
Army Missile Command
Redstone Arsenal, Alabama

APPENDIX B-1

PRELIMINARY PURCHASE DESCRIPTION

SHELTER MULTISYSTEM TEST EQUIPMENT

APPENDIX B-1

PRELIMINARY PURCHASE DESCRIPTION

SHELTER MULTISYSTEM TEST EQUIPMENT

This shelter purchase description is composed of Specification MIL-S-52059A (Sig C), dated 25 September 1961, and the following sheets.

EXCEPTIONS (Referenced to paragraph numbers of Specification MIL-S-52059A):

1.1 Delete and substitute: "This specification covers three (3) types of light-weight field and mobile shelters designed for transport by cargo truck, fixed or rotary winged aircraft, rail, ship and landing craft and designated as shown in paragraph 1.2."

1.2 Classification. - Add new paragraph: The shelter covered by this specification shall include the classes specified in the following table:

SHELTER CLASSES

Class	Designation
1	Shelter, Electronic Test Unit 1
2	Shelter, Electronic Test Unit 2
3	Shelter, Hydraulic Test Unit

2. Applicable documents. - Add the following documents:

DRAWINGS

Ordnance Corps

____________	Shelter, Class 1
____________	Shelter, Class 2
____________	Shelter, Class 3

SPECIFICATIONS

Military

MIL-A-8421B (USAF)	Air Transportability Requirements, General Specification For Dated 5 May 1960

PURCHASE DESCRIPTIONS

MTE-5710	Environmental and Service Conditions, Multisystem Test Equipment
Inspection Equipment List	
IEL	Shelter, Class 1
IEL	Shelter, Class 2
IEL	Shelter, Class 3
Packaging Data Sheets	
MIL-G- ________	Shelter, Class 1
MIL-G- ________	Shelter, Class 2
MIL-G- ________	Shelter, Class 3

STANDARDS

Federal Standard No. 595	Colors

3.1 Shelter construction. - Delete the first sentence and substitute: "Shelter, Class 1, 2, and 3 as described in paragraph 1.2, shall be a rectangular shaped configuration as shown in Ordnance Corps Drawings ________ , ________ , and ________, respectively."

3.1.1 Overall dimensions. - Delete the first sentence and substitute: "The overall dimensions for each class of shelter shall be as specified in the following list:

Length	--	163	inches (max.)
Width	--	83 1/2	inches (max.)
Height	--	87	inches (max.)

The inside overall dimensions for each class of shelter shall be as specified in the following list:

Length -- 152 inches (min.)

Width -- 76 inches (min.)

Height -- 79 inches (min.)."

3.1.2 Shelter weight. - Delete the first sentence and substitute: "The gross weight of each class of shelter shall not exceed 1500 pounds."

Delete paragraph 3.4.1 and substitute the following:

3.4.1 Skids. - A minimum of two skids shall be mounted longitudinally on the under-surface of the shelter. These skids shall permit the shelter fully equipped with a payload of 6500 pounds to be towed over a hump formed by a ramp and its platform without signs of damage, deterioration, and structural deformation as a result of such towing. The design of the skids shall be compatible with the loading requirements of C123B aircraft and M55 military cargo trucks. No permanent deformation shall occur to any part of the shelter when the shelter is balanced or pivoted anywhere along the skids on a 2-inch diameter pipe.

Shock absorbent skids, similar to Ordnance Part Number 10641000, shall be installed in accordance with Installation Drawings. These skids shall be designed to limit shock applied upward to the floor of the shelter to no more than 10 g of 30 $\pm$ 1 milli-second duration. There shall be no degradation of the shelter capability of being towed in any direction or turned while being towed. Skids having different load absorbing capabilities according to the description of the load within the shelter shall be acceptable.

3.4.2 Towing eyes. - Substitute "type C123B" for "type C119." Substitute "type M-55" for "type M-35."

Delete paragraph 3.5 and substitute the following:

3.5 Door and doorway. - The doorway shall be located in the end walls in accordance with the Installation Drawings for each class. Doors shall be 30 inches plus or minus 1/8 inch wide and 82 inches plus or minus 1/4 inch high; they shall be on radii of not more than 2-3/8 inches. Doorways shall be located on end panels in

accordance with the Installation Drawings for each class. The door shall consist of an upper and lower section sealing the doorway. To provide for the cover and air filter specified in paragraph 3.8.1, an opening having nominal dimensions of 15-13/16 inches by 10-13/16 inches shall be fitted in the lower half of the upper section of the door. The door shall open outward.

3.6.3 Escape hatch. - Add new paragraph: The shelter shall be equipped with one rectangular escape hatch in accordance with the applicable drawing. The hatch door shall open inward.

Delete paragraph 3.8 and substitute the following:

3.8 Ventilation. - The cooling of equipment contained within the shelter shall be accomplished by the circulation of outside air, together with the re-circulation of inside air, by one or more external air conditioners in accordance with the applicable drawings. An air outlet and filter opening shall be provided in the door of nominal dimensions of 15-13/16 inches wide by 19-13/16 inches high. A cleanable metal filter, rated at 3 cfm per square inch of area, shall be provided. A gasketed outside hinged weather cover which can be held open by a captivated wing screw shall also be provided. This filter assembly shall be light-proof and drip-proof when the cover is in the open position. A stenciled note shall be put on the exhaust outlet cover directing that it be kept open during air transportation. Air inlet ports in the shelter walls shall be fitted with hinged weather covers in the same manner as for the air exhaust port.

3.8.1 Inlet. - Delete.

3.8.2 Exhaust. - Delete.

3.11 Drops. - Substitute "6500 pounds" for "5000 pounds."

3.15.1 Air transportability (rotary wing aircraft). - Substitute "6500 pounds" for "5000 pounds."

3.15.2 Rail transport. - Substitute "6500 pounds" for "5000 pounds."

Delete paragraph 3.15.3 and substitute the following:

3.15.3 Vehicular transportation. - The shelter with a payload of 6,500 pounds shall be capable of being transported over cross-country terrain by M55 military cargo truck.

3.15.4 Dolly transportability. - Add new paragraph: The shelter shall have provisions on the basic structure for attaching cantilever-type dollies meeting Type III Mobility Requirements as defined in MIL-M-8090. The attachments shall be of such strength to permit carrying of the shelter with maximum payload.

Delete the paragraph 3.17 and substitute the following:

3.17 Loading, handling, and tiedown provisions: The shelter shall have provisions for the following:

a. Attachments and operation of a loading and handling device. Attachments for such a device shall be made along the four vertical corner members and shall be of appropriate strength and design as to permit raising the shelter to a point where it can be loaded on an M55 cargo truck.

b. A minimum of four tiedown points shall be provided which are adequate for securing the shelter when transported by M55 cargo truck, C123B aircraft, and by rail. Such points of attachment may be adjacent to and integral with lifting eyes specified in paragraph 3.6.1. Tiedowns shall be capable of withstanding an 8g shock when applied longitudinally to the shelter as in aircraft emergency landing procedures.

3.19 Delete the following: . . . . . and Drawing SC-A-47784.

3.23.3 Aircraft Loading Data Plate. - Substitute "Specification MIL-A-8421B" for "SGD-82768."

3.23.6 Instructions. - Add the following item:

d. The attachment and operation of jacks, dollies, and transporter.

3.25 Securing of parts. - Substitute "shelter" for "equipment" throughout the paragraph.

Delete paragraph 3.30.2 and substitute the following:

3.30.2 Machine screws, cap screws, and washers. - Machine screws, cap screws, and washers shall be corrosion resistant.

3.32 Lift and tiedown provisions. - Substitute "M-55" for either M-35 or M-211 and delete ... and shall conform to Dwg SC-D-36423.

3.33.3 Elevation. - Substitute "50,000 feet" for "25,000 feet."

Delete paragraph 3.33.4 and substitute:

3.33.4 Rain. - Shelters shall be designed to withstand the following 24-hour rain cycle: 32 inches of rainfall, with winds up to 40 miles per hour.

3.33.5 Blackout. - Add new paragraph: Provision shall be made for the installation of protective blackout curtains within the shelter at the doorway. Suitable interlocks shall be provided to the shelter electrical system so that the lighting system may be disabled when a door is opened with a suitable low intensity alternate light source being switched on. An override for the provision shall be installed.

4.6 Maximum weight inspection. - Substitute "1500 pounds" for "1200 pounds."

4.14 Three-point suspension test. - Revise as follows: The shelter with a 6,500 pound payload per Drawing ___________ shall be supported on the ground by any three corners to determine compliance with paragraph 3.18.

4.15 Skid bearing test. - Substitute "6500 pounds" for "5000 pounds."

4.16 Towing test. - Substitute "6500 pounds" for "5000 pounds."

4.18.1 Airflow Reduction. - Delete.

4.19.2 Sling drop. - Substitute "6500 pounds" for "5000 pounds."

4.20 Static Load Test - Cargo Handling. - Substitute "22,750 pounds" for "17,500 pounds."

4.21.1 Railroad humping. - Delete the first sentence and substitute the following: the shelter shall be loaded with a 6500 pound payload per Drawing

__________ and shall be loaded in a manner normally used for shipment on a railroad car.

4.21.2 Military truck transport. - Substitute "6500 pounds" for "5000 pounds."

4.21.3 Flat drop. - Substitute "6500 pounds" for "5000 pounds."

4.25 Altitude test. - Substitute "50,000 feet" for "25,000 feet."

4.27 Rain test. - Qualify as per Specification MTE-101.

4.27.1 Delete.

4.27.2 Delete.

4.27.3 Delete.

4.27.4 Delete.

4.27.5 Delete.

4.27.6 Delete.

4.27.7 Delete.

4.27.8 Delete.

4.28 Visual and mechanical inspection. - Revise Table V by adding the following:

Class	Defect
Minor	Keys do not operate locks.

5.1 Delete, "5-1H1( )/G" in this paragraph and replace with a blank "__________."

6.1 Ordering Data - Delete SC-C-33073 in paragraph (2) d. and replace with a dash.

NOTICE: When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated,

furnished, or in any way supplied the said drawings, specifications, or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

CUSTODIAN:	PREPARING ACTIVITY:
Army-Ordnance Corps	Army Missile Command Redstone Arsenal, Alabama

APPENDIX B-2

SWITCHING CONTROL LANGUAGE

APPENDIX B-2

SWITCHING CONTROL LANGUAGE

Each unit or function to be controlled by the switching control buffer is addressed by a three character (Fieldata) mnemonic address which represents the major function of the unit. The unit to be controlled may have more than one internal function. To identify the different internal functions, a single character mnemonic representation of the function is used as a subaddress.

The range/value data to be transferred to the controlled unit consists of decimal information. This data is coded as a 4-bit BCD character. The number of decimal characters required to control the unit is transferred as that many sets of BCD characters.

The present complement of switching control addresses is as follows:

Address	Unit or Function Addressed
LBC	L-Band carrier frequency
XBC	X-Band carrier frequency
LRA	L-Band Ratiometer attenuator
XRA	X-Band Ratiometer attenuator
LCA	L-Band unmodulated carrier attenuator
XCA	X-Band unmodulated carrier attenuator
LMA	L-Band modulated carrier attenuator
XMA	X-Band modulated carrier attenuator
LBM	L-Band modulation type
XBM	X-Band modulation type
AC4	AC Voltage- 400 cps 3 phase
AC8	AC Voltage- 800 cps 3 phase
ACS	AC Voltage-Single phase
DC1	DC Power Supply #1
DC2	DC Power Supply #2

Address	Unit or Function Addressed
DC3	DC Power Supply #3
DC4	DC Power Supply #4
DC5	DC Power Supply #5
DCH	DC Power Supply-(High Voltage)
DCM	DC Power Supply-(Medium Voltage)
DA1	DACON #1
DA2	DACON #2
DA3	DACON #3
DA4	DACON #4
DA5	DACON #5
DA6	DACON #6
DA7	DACON #7
VLF	Very Low Frequency Generator
AFG	Audio Frequency Generator
RFS	RF Synthesizer
RFA	RF Attentuator
FSO	Frequency Standard Output
PCA	Variable Phase Converter/Amplifier
RES	Resistive Load Assembly
PGN	Pulse Generator
PAI	Pulse Power Amplifier-Internal Control
PAE	Pulse Power Amplifier-External Control
DMG	Digital Message Generator
DMR	Digital Message Receiver
AFS	DC/AF Switch
SOR	Stimulus Output Routing
MDB	Measurement Data Buffer
STM	Self-Test Monitor
TPA	Test Point-A-Bus
TPB	Test Point-B-Bus
MFN	Measure frequency-normal range
MFE	Measure frequency-extended range
MTS	Measure time interval-single channel
MTD	Measure time interval-dual channel

Address	Unit or Function Addressed
MAC	Measure AC Voltage
MDC	Measure DC Voltage
MRE	Measure Resistance
MRF	Measure RF Voltage

APPENDIX C

COMPUTER/CONTROLLER FUNCTIONAL DESCRIPTION

C.1 INTRODUCTION

This is a revised and updated description of the Computer/Controller Group description contained in Appendix A of the third Quarterly Interim Technical Report.

C.2 DESCRIPTION

A revised Computer/Controller block diagram is shown in Figure C-1. It differs from that given in the third Quarterly in the following ways:

(a). The diagram has been compartmentalized to highlight the major building block functions of Computer, Controller, Peripheral, and Display/ Control.

(b). The peripheral device control functions were concentrated into one assembly known as the Peripheral Control Assembly.

(c). The punch and its control were removed in accord with TDO-20. This TDO also eliminated the "Write on Magnetic Tape" capability of the system.

C.2.1 FUNCTIONAL UNITS

The functions of each of the units of the Computer/Controller are described in the following paragraphs.

A. Memory Assembly

The Computer/Controller rises as its high-speed storage unit, a random-access, coincident-current, expandable magnetic-core memory. It has 4096 addressable word locations. The cores utilized in this memory are the wide temperature range RCA Type 0066M5 developed specifically for military applications.

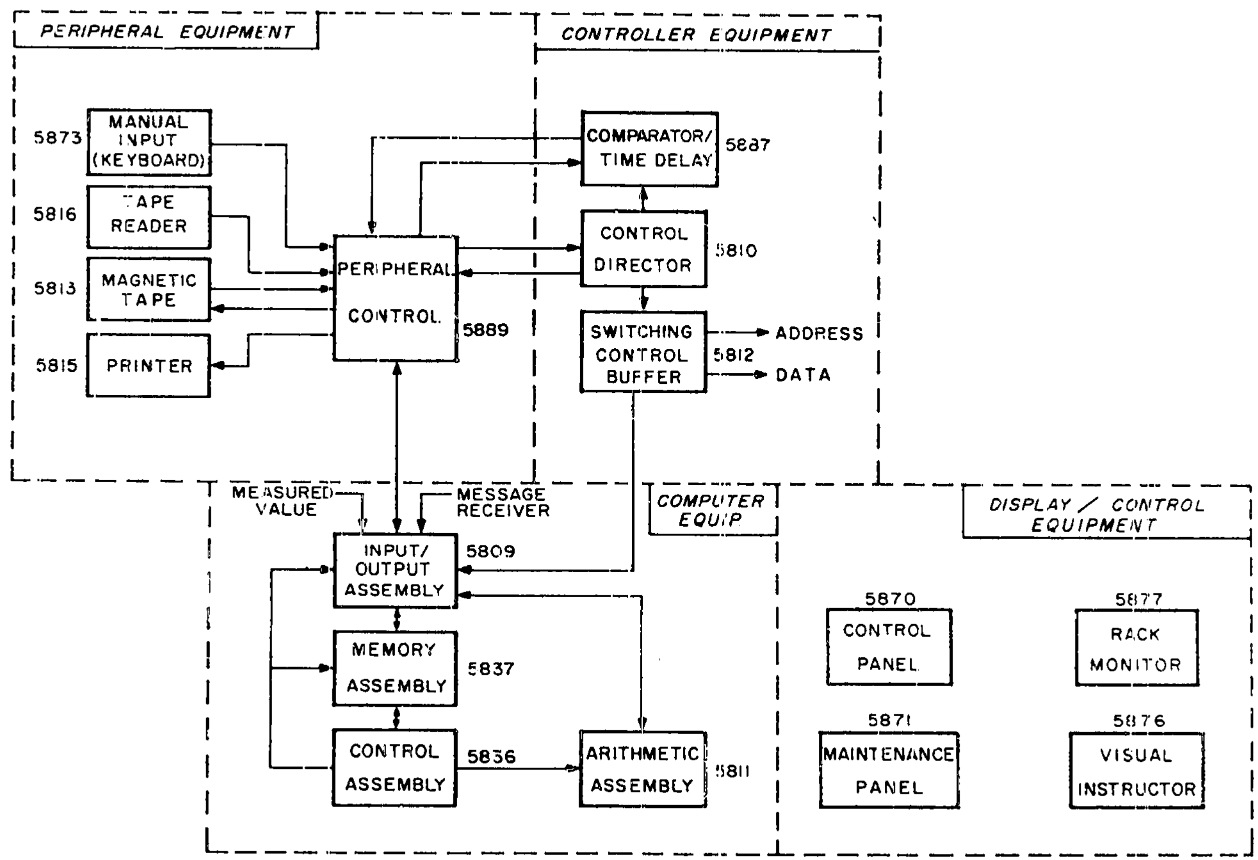

Figure C-1. MTE computer/controller block diagram

A word contained in the memory consists of 24 bits plus one parity bit. It may be either an instruction or a data word. An instruction word contains an operation code, a set of index register indicators, and an address. The address part is used to denote the location in the memory containing a word which is to be subjected to some arithmetic or logical operation. The operation code is used to specify the instruction to be performed, and the index register indicators select one of three index registers. In the instruction word format the most significant six bits contain the operation code; the next three bits select the index registers; there are three spare bits; and the remaining 12 bits are the address.

Although the programmer has freedom to adopt many conventions in his choice of number systems, the usual interpretation of numbers within the MTE computer is that all numbers lie within the range $+1 \geq x \geq -1$. Under this convention the most significant bit is regarded as the sign bit; the machine point comes after the sign bit, and the remaining 23 bits indicate the magnitude. A zero in the sign bit means the number is negative. A negative number is represented in two's complement form. This convention results in an unambiguous zero.

The memory cycle time is 12 microseconds, i. e. it takes a total of 12 microseconds: (1) to address a particular memory location, (2) to strobe its contents, (3) to read its contents, and (4) to restore its original contents.

This process is accomplished under control of the memory timing section. Memory input/output operations are accomplished via a 24-stage parallel memory register. Input/output rates up to 83, 333 words per second are possible.

B. Arithmetic Assembly

The arithmetic assembly consists of an accumulator, a quotient register and adder logic. With these functions the computer can perform three basic arithmetic operations: (1) add the contents of a specified memory location to the contents of the accumulator, (2) complement the contents of the accumulator, and (3) shift the contents of the accumulator and the quotient register (Q)

right or left. All other arithmetic and logical functions are built on the framework of these three elementary capabilities. Subtraction of the memory contents from the accumulator is accomplished by complementing the accumulator and adding to it the memory register contents. For multiplication, the multiplier is placed in the Q register and the multiplicand in the M register. The instruction is implemented by a repeated cycle in which the multiplicand is added to the accumulator contents to form a partial product which is then shifted to the right. A double-length product is formed in the accumulator and Q registers. In division, the divisor contained in the memory register is subtracted repeatedly from the double length dividend or remainder in the accumulator and Q registers, the remainder being shifted left after each step. The quotient is formed in the Q register. The number of status level changes that occur in the multiplication and division instructions and in the shift instructions is controlled by a four-stage loop counter.

C. Control Assembly

The control assembly consists of an operations register, time-pulse generator, and the command and status level generators. These functions store and interpret the instructions of the computer and direct the sequence of operations of the computer.

When an instruction word is read from memory it is temporarily stored in a memory output register. Interpretation of the instruction contained in the memory register is started by transferring the operation code contained in the six most significant stages of the memory register to the six-stage operation (O) register.

Outputs from the operation (O) register are combined with outputs from the timing generator to control selected stages of the status level generator. The contents of this register delineate major subdivision of the instruction or status level.

The content of the operation (O) register also is decoded by the operation decoder. Outputs from the decoder, combined with those from the time-pulse

generator and the status-level generator, operate logic in the command generator to energize the command lines in an ordered sequence required for the implementation o a particular instruction.

Each required command exists for a basic time of 0.5 microseconds (determined by the time pulse generator) and effects one elementary transfer or arithmetic operation. For example, one command transfers the contents of the lower accumulator to the upper Q register; another transfers to the operation register from the most significant stages of the memory register.

When all the commands for a particular instruction have been generated, the command generator provides a pulse to the memory timing to initiate the readout process for the next instruction word.

D. Input/Output Assembly

The input/output assembly performs two main functions: (1) it is the input/output interface with the computer; and (2) it is the memory input/output facility along with the parity logic.

The computer input/output assembly consists of a register and the necessary routing gates to receive and transmit computer words from and to all necessary external devices. The data to be sent to the computer is assembled into computer format external to the computer and routed to the input/output register through the appropriate control gates. The computer can accept information in this manner up to an 80-kc rate on words up to 24 bits in length. The output capability is included to extract data in a 24-bit parallel fashion or a 6-bit parallel fashion, in this manner simulating a Fieldata output for peripheral devices.

Incorporated with the input/output function is an interrogation feature. This allows the computer to continue on an internal program if the external device using the previous piece of data has not yet completed its operation.

The memory input/output logic serves as the routing gate(s) and the temporary storage for information going to and coming from the memory. The logic con-

sists of two registers and the memory parity checking circuits. Each word to be stored into the memory is tagged with the parity bit; upon readout the parity is re-checked to ascertain validity of the word.

E. Magnetic Tape Assembly

The magnetic tape assembly is controlled by the computer, via the peripheral control assembly, by the use of Read instructions under control of the program. The tape assembly is automatically controlled and searched for the desired test program upon selection by the operator.

When reading magnetic tape, the Read instruction includes the memory location for loading the first word. Sequential memory addresses are used for each subsequent word until the instruction execution is terminated by sensing a unique character indicating end of data. The data from the magnetic tape unit is scanned for odd parity; a parity error terminates the tape reading process and a "Halt-Computer/Controller" command is generated. Prior to executing the Read instruction, the tape is searched for the desired block of data whose address has been previously specified.

F. Perforated Tape Reader

The perforated tape reader sequences blocks of information into the computer. A "Read Perforated Tape" instruction automatically provides a start command to the reader. The first tape character sets up the mode decoder to select one of two input modes: octal, or alpha-numeric. The control director and switching control assemblies then proceed to assemble a 24-bit word from the input characters as directed by the mode decoder. For an octal input, eight 3-bit units are packed into the 24-bit memory word; for the alpha-numeric mode, four 6-bit characters are packed into the 24-bit word. In the event that a parity error is sensed, a parity error display on the operator's console will illuminate; the computer will halt without storing the word with incorrect parity.

G. Control Director

The control director controls the operations of the printer, comparator/time delay, switching control buffer, and other automatic test functions. The control director receives data serially by character from the computer via the input/output assembly under a Write instruction. It interprets the instructions contained within the data and issues appropriate commands to other units. The control director performs these functions by generating the timing pulses and status levels necessary to store, decode, and carry out the operations described by the instructions contained in the data from the input/output assembly.

The control director may also receive data from the manual input, as well as from the input/output assembly. The operations of the control director, in this mode, are the same as when data is received from the computer via the input/output assembly.

H. Printer

The printer operates under the direction of the control director. The peripheral control is addressed by the control director when a Print instruction is programmed in the data from the computer. The print format is under the control of the output Fieldata characters, (following the Print instruction) that are sent to the printer. Synchronizing pulses between the printer, control director, and the computer are provided.

I. Peripheral Control

The peripheral control assembly provides the logical and electrical interface between the controller and the input-output devices. Input information may come from the manual input, the tape reader, the magnetic tape assembly, or the input/output assembly. Incoming information feeds into the peripheral control from the various input devices, then is fed out of the peripheral control in a character serial, bit parallel fashion onto an information bus which goes to the control director.

Output information is handled by the peripheral control unit in the inverse fashion. A character bus feeds information from the control director to the peripheral control in a character serial, bit parallel manner. The output information is then fed from the peripheral control to the selected output unit. Output devices include the printer, and the magnetic tape assembly.

J. Comparator/Time Delay

This assembly operates under the direction of the control director and is composed of a comparator with its associated control and input select functions and a counter which performs time delay functions.

The comparator is utilized to (1) determine if the measured value is within limits and (2) locate the desired block of data on tape. When performing limit comparisons, the comparator compares the measured value from the measurements section versus the upper and lower limits received over the single character data bus. If the measured value is greater than the upper limit, a HIGH output is indicated; if less than the lower limit, a LOW output is indicated; and if between the two limits, a GO is indicated.

When the Computer/Controller is performing tape search operations, the comparator determines if the desired address is greater than, equal to, or less than the address for each particular block of data on tape. If greater than, a tape forward output is indicated; if less than, a tape reverse output is indicated; and if equal to, an address output OK is indicated, and data from tape is allowed to be read into the system.

The time delay can be programmed to interrupt the Computer/Controller operations for one microsecond to 166 minutes or it can be programmed to measure elapsed time in the above range while other operations are being performed.

The time delay function can be utilized to synchronize the automatic test system operation with that of a unit under test, by programming the start

of a delay to be controlled by the UUT and by allowing the UUT to control the magnitude of the time increments. When the delay is started by the UUT, a measurement of the selected UUT test parameter is automatically made when the delay is completed.

K. Switching Control Buffer

The switching control buffer provides the temporary storage and decoding of the switching words which specify the selection and ranging of all stimulus and measurement devices. The signal routing and test point selection are also controlled by unique switching words. The switching control buffer is addressed by the control director when a Switching Follows instruction is programmed in the data received from the computer via the input/output assembly. Each switching word (composed of a variable number of characters) following the Switching Follows instruction is temporarily stored in the switching control buffer until its specified control operations are performed.

L. Controls and Displays

Facilities will be provided so that the operator and/or maintenance technician may meaningfully communicate with the computer/controller. Some of the facilities provided will be used mainly for computer checkout and maintenance rather than operation; the most desirable layout for these facilities has been determined by human engineering.

The maintenance philosophy for automatic test systems is that displays will be provided on the control console which will indicate which major unit is malfunctioning. Displays will also be provided on each unit to indicate the status of major functions contained therein. Therefore, the operator's control console will contain only those displays required for normal operation and those which indicate the status of the major units.

The following controls and displays are located on the control console:

a. Visual Instructor

The visual instructor is a microfilm reader which is used to display schematic diagrams, component layouts, unit under test hookup connections, and special pictorial repair instructions.

b. Control Panel

The control panel contains the controls which require operator participation during this testing of a unit under test and the displays which inform the operator of the status of the testing routine. Where indicated, the functions listed below are both controls and displays which give positive indication of the selected control and status.

1. Unit Under Test Address Number - Six rotary "digi" type switches select the UUT address number (0000 to 9999) and the test number (00 to 99) at which to start test of the unit under test. (Control and Display)
2. Automatic Test Mode - Selects the automatic test mode of operation and starts the test system operations of the functions of this mode. This mode removes any previously selected mode or submode of operation. (Control and Display)
3. Standby Pushbutton - Stops the test system operation, removes any previously selected mode, and resets the complete test system to initial conditions. (Control and Display)
4. Program Interrupt Pushbutton - Interrupts the test system operation at the completion of the existing instruction. (Control and Display)
5. Proceed Pushbutton - Initiates program continuation from the point at which the test system operation had been previously interupted.
6. Print All/Print NO-GO Only Pushbutton Switch - Selects whether each measurement result will be printed or whether only the NO-GO measurement results will be printed. (Control and Display)
7. Continuous Conversion Pushbutton - Interrupts the test system operation each time that an Evaluate instruction is recognized and causes repeated measurements of the selected parameter. (Control and Display)

8. Reset Pushbutton - Resets all of the computer/control circuits to their initial condition.
9. Switching Reset Pushbutton - Allows the operator to reset all switching previously set up for the stimulus and measuring devices.
10. Time Delay in Progress - Single display which is illuminated whenever the test system is instructed to perform a time delay.
11. Parity Error - Illuminates whenever a parity error is detected within the computer/controller.
12. Switching Verification Error - Illuminates whenever a switching verification is not achieved.
13. Measurement in Progress - Single display which is illuminated when the test system is performing a measurement.
14. Start Pushbutton - Starts the test system operations of the mode selected by the Mode Switch.

c. Maintenance Panel

The maintenance panel contains the controls and displays provided as an aid to the operator in maintaining the test system.

1. Mode Switch - This six position switch places the computer/controller in the Automatic Test, Magnetic Tape to Memory, Paper Tape to Memory, Memory Test, Paper Tape Test, or Manual Test mode of operation.
2. Computer Submode Switch - This three-position switch places the computer in the Normal, Single Computer Instruction, or Single Clock submode.
3. Controller Submode Switch - This three-position switch places the controller in the Normal, Single Controller Character, or Single Controller Pulse submode.
4. Memory Mode Switch - This three-position switch places the computer in the Run, P-Count, or Interrupt Address mode. The Run position is the normal operating position. The P-Count position allows the computer to advance the program counter to an address

specified by the Interrupt Address Switches without performing any instructions. The Interrupt Address position allows the computer to perform the instructions of the program and then to stop the program at an address specified by the Interrupt Address Switches.

5. Interrupt Address Switches - Four rotary "digi" type switches select the memory address (0000-7777) at which the computer operation will be stopped. (Control and Display)
6. Instruction Display - Displays the instruction under which the computer and/or controller is currently operating.

d. Manual Input

The manual input consists of a keyboard which allows the operator to manually control the operation of the controller when in the Manual Test mode of operation. From this keyboard the operator can insert any desired controller test sequence a character at a time as well as punch on the paper tape punch any desired set of Fieldata characters.

APPENDIX D

INTERRELATIONSHIP OF THE SWITCHING CONTROL BUFFER (5812) WITH THE TIME INTERVAL AND FREQUENCY METER (5777)

For the Time Interval and Frequency Meter the frequency measurements will be controlled by a switching word of the following format:

Address	SD1	SD2	SD3
MFN	Time Base	Trigger Level	Time Period Average
MFE	Time Base	Trigger Level	Time Period Average

MFN sets up a frequency measurement in the normal range of 20 cps to 10Mc. MFE sets up a frequency measurement in the extended range of 10 Mc to 100 Mc. SD1 (Switching Data Character No. 1) is the first BCD character. The following BCD table will be used for the above format:

BCD	SD1	SD2	SD3
0	10^{0} sec		1 period avg.
1	10^{-1} sec	-0.05 volts	10 period avg.
2	10^{-2} sec	+0.05 volts	
3	10^{-3} sec	0.5 volts	
4	10^{-4} sec	+0.5 volts	
5	10^{-5} sec		
6	10^{-6} sec		
7	10^{-7} sec		
8	10^{+1} sec		
9			

Time interval mea urements will be controlled by a switching word of the following format:

Address	SD1	SD2	SD3	SD4	SD5
MTS	Time Base	Start Trigger Level	Start Slope	Stop Trigger Level	Stop Slope
MTD	Time Base	Start Trigger Level	Start Slope	Stop Trigger Level	Stop Slope

MTS sets up a time interval measurement on a single channel (A Bus). MTD sets up a time interval measurement on dual channels (Start on A Bus, Stop on B Bus). The following BCD Table will be used for the above format:

BCD	SD1	SD2	SD3	SD4	SD5
0	10^{0} sec				
1	10^{-1} sec	-0.05 v	-	-0.05 v	-
2	10^{-2} sec	+0.05 v	+	+0.05 v	+
3	10^{-3} sec	-0.5 v		-0.5 v	
4	10^{-4} sec	+0.5 v		+0.5 v	
5	10^{-5} sec				
6	10^{-6} sec				
7	10^{-7} sec				
8	10^{+1} sec				
9					

The control lines between the Time Interval and Frequency Meter and the Switching Control Buffer will be as follows:

4 Address lines
4 Timing pulse lines
1 Apply signal line
1 Reset signal line
1 Verification signal line
11 signal lines total
20 Switching Data lines
31 control lines total

The control hardware for the Time Interval and Frequency Meter will include three character storage boards and one address board of the 3 subaddress type.

APPENDIX E

FUNCTIONAL DESCRIPTION OF THE COMPARATOR/TIME DELAY (5887)

E.1 TIME DELAY

The time delay has three inputs: (1) the data bus, (2) time bases (1 Mc, 1 kc, 1 cps and external); and (3) control lines. The time delay assembly consists of a 4-decade countdown counter that is preset by decimal digits received serially over the data bus. The preset action is accomplished under the direction of the Control Director whenever a Delay Magnitude (D) instruction is programmed.

When the Control Director decodes the Time Start instruction, it sends this information to the Comparator/Time Delay Unit (C/TDU) to initiate the count. At the end of the count, the C/TDU sends the Control Director an End of Time Count signal, thus indicating the end of the delay whose magnitude was preset in the counter. This delay may be in microseconds, milliseconds or seconds according to the time base selected.

Under an External Start instruction, the Control Director sends the C/TDU an External Start Signal. The C/TDU then prepares itself to start the count whenever an external (UUT) signal is received. At the end of the count, the measurement unit is commanded to perform a measurement.

In establishing the time bases and the length of the counter to be utilized in the time delay function, the following factors were considered:

1) Available frequencies
2) Accuracy
3) Minimum delay required
4) Maximum delay

There are a number of frequencies available in the MTE system; however, due to the requirement to program the magnitude of the time delay in the familiar decimal form, only those frequencies which are multiples of the base 10 system were considered. These frequencies were readily available from the Measurements Group in the range from 0.1 cps to 10 Mc (10 sec, 1 sec, 100 millisec, 10 millisec, 1 millisec, 100μ sec, 10μ sec, and 0.1μ sec). Of these time bases it was preferable from the programming viewpoint, to utilize only those which allow the magnitude of the time delay to be written directly. These were the 1 second, 1 millisecond, and 1 microsecond time bases.

An accuracy of at least one percent was desired. A 2-decade counter would have yielded the one percent, however, this accuracy would be only at full scale (count of 99). By utilizing a 4-decade counter, the 1-percent accuracy could be obtained over three fourths of the scale. This was considered adequate. The minimum delay required was on the order of microseconds and the maximum delay was around 900 seconds (15 minutes). A 4-decade counter and time bases of 1 microsecond, 1 millisecond, and 1 second provide delays from microseconds to 9999 seconds.

E.2 LIMIT COMPARISON

When a limit comparison is being performed, the data bus serves as one input of the assembly and the measurement output buffer serves as the second input.

Under a Compare Upper instruction, the Control Director decodes the instruction and sends a command (U) to the comparator. The 4-bit parallel comparator then compares the upper limit value from the data bus (DB) with the measurement value (MV) one character at a time. The outputs b ($|MV| > |DB|$) and e ($|MV| = |DB|$) indicate absolute comparison of the corresponding characters.

A sign determination of both numbers (the sign of the measured value (SV) and the sign of the limit (SB)) is performed and stored.

The decision logic assembles these inputs, determines the final result, and provides outputs (HI indicating MV>DB or GO indicating MV $\leq$ DB) to other units.

Under a Compare Lower instruction, the Control Director decodes the instructions and sends a command (L) to the Comparator. In a similar way, the results (LO indicating MV<DB or GO indicating MV$\geq$DB) are obtained and are provided as outputs to other units.

Under two consecutive instructions, U and L (or L and U) the results are HI LO, GO as a combination of both cases.

The basic Boolean equations implemented (timing signals excluded) are:

$$HI = U\,(b \cdot SV \cdot SB + \overline{b} \cdot \overline{SV} \cdot \overline{SB} + SV \cdot \overline{SB}) \cdot \overline{CI}$$

$$LO = L\,(b \cdot \overline{SV} \cdot \overline{SB} + \overline{b} \cdot SV \cdot SB + \overline{SV} \cdot SB) \cdot \overline{CI}$$

$$GO = \{U\,(b \cdot \overline{SV} \cdot \overline{SB} + \overline{b} \cdot SV \cdot SB + \overline{SV} \cdot SB) + L$$
$$(b \cdot SV \cdot SB + \overline{b} \cdot \overline{SV} \cdot \overline{SB} + SV \cdot \overline{SB}) + e\} \cdot \overline{CI}$$

where

$b \equiv |MV| > |DB|$
$\overline{b} \equiv |MV| \leq |DB|$
$SV \equiv$ sign of the measured value is positive
$\overline{SV} \equiv$ sign of the measured value is negative
$SB \equiv$ sign of the limit is positive
$\overline{SB} \equiv$ sign of the limit is negative
$e \equiv |MV| = |DB|$
$CI \equiv$ comparison inhibit (further comparisons against a limit are inhibited whenever a result HI, LO or GO are obtained)
$\overline{CI} \equiv$ comparison is not inhibited

At the end of the comparison the C/TDU sends a Comparison Finished (CF) signal to the Control Director.

E.3 TAPE SEARCH

The Tape Search operation uses the same circuitry as that of limit comparison with minor additions. The data bus is fed to the 4-bit parallel comparator as one input and the Data Address Register and UUT Program Number as the other input.

When a Tape Search operation is in process, the data from the tape is scanned for the desired address. Each address on the tape is keyed before and after by an Address Follows Instruction (AF). This gives the system the capability to search for data on tape either in the forward or reverse direction. Upon recognition of each AF instruction, a signal (AF) is sent to the C/TDU. This signal initiates the comparison routine between the address from tape and the desired address (UUT Program Number and the Data Address).

Precautions are taken to assure that the appropriate data from tape is interpreted by the comparator. This is necessary due to the keying of the addresses before and after. The addresses are always fixed in length; therefore, when searching the tape either in the forward or reverse directions, the first AF instruction recognized starts the comparison routine and the second AF instruction recognized stops the comparison. If the second AF is not a certain fixed length from the first, the comparator knows that it started comparing on the AF instruction which followed the address, and not on the one which preceded it. Therefore, the comparison is ignored and the next AF instruction recognized will again start the comparison routine. This next AF instruction will always be the one which precedes the address.

The addresses or tape are programmed most significant digit first, as scanned in the forward direction. When scanned in the reverse direction, the addresses are received least significant digit first. The Decision Logic, in conjunction with the Routing Multiplexer, of the C/TDU is designed to handle both cases.

The operations of the C/TDU during Tape search are shown in the flow chart of Figure E-1. The search is started when the Control Director sends a start signal (J) to the C/TDU.

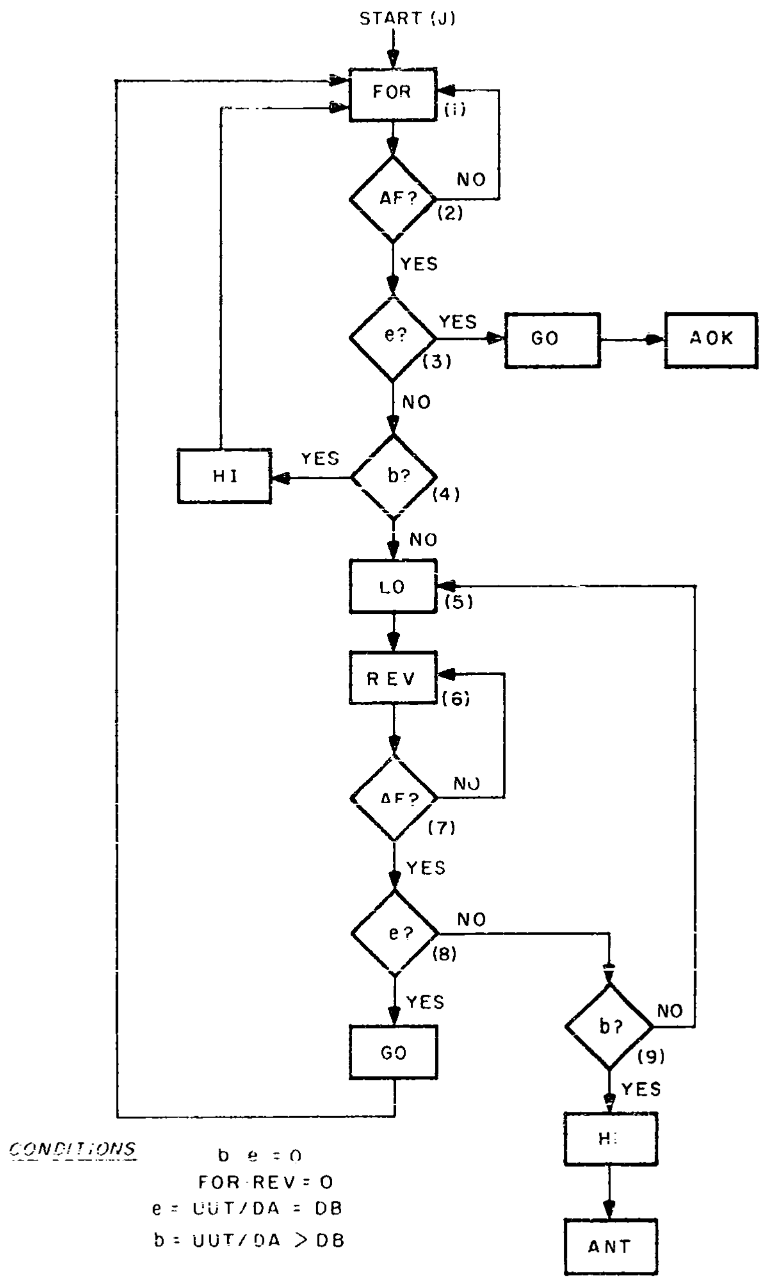

Figure E-1. Search flow chart

Block 1 - The tape is started in the forward direction

Block 2 - Is the character from tape an AF instruction. If no, continue in the forward direction; if yes, compare.

Block 3 - If the comparator output is e (indicating that the addresses are equal), a GO and address OK are generated, and the data from tape is read into the system. If not e, go to Block 4.

Block 4 - If the output from the 4-bit comparator is b, indicating that the address searched for is ahead, an output HI is obtained and the tape continues moving in the forward direction. The processes of Blocks 1 through 4 are repeated until an e is obtained. If the output from the comparator was not b, indicating that the desired address is in the other direction on the tape, go to Block 5.

Block 5 - Not b indicates a LO output.

Block 6 - The tape motion shall be in the reverse direction.

Block 7 - Is the character from tape an AF instruction. If no, continue in the reverse direction; if yes, compare.

Block 8 - If the comparator output is not e, indicating that the addresses are not equal, go to Block 9. If the comparator output is e, indicating that the addresses are equal, go to Block 1. The tape is then searched in the forward direction, until the desired address is located. The data is then read into the system while the tape is moving in the forward direction. (Data must always be read into the system during forward tape motion, as this is the order in which data is programmed.)

Block 9 - If the comparator output is not b, indicating that the desired address is still in the reverse direction, return to Block 5 and continue the search process. If the comparator output was b, then the addresses on tape are not in sequence or the desired address is not on the tape (ANT) and the system is stopped.

The logic of tape search is implemented with the same circuitry used in limit comparison. The basic Boolean equations (timing not included) are:

$$HI = J \cdot CS \cdot b\,(FOR \cdot \overline{CI} + REV)$$
$$LO = J \cdot CS \cdot \overline{b}\,(FOR \cdot \overline{CI} + REV)$$

$$GO = e \cdot \overline{CI}$$

$$FOR = AF \cdot CS \cdot GO$$

$$REV = AF \cdot CS \cdot LO$$

$$AOK = GO \cdot CS \cdot AF \cdot FOR$$

$$ANT = REV \cdot HI$$

where

J	$\equiv$	Search command
CS	$\equiv$	Comparison in Search Mode
b	$\equiv$	UUT/DA > DB
$\overline{b}$	$\equiv$	UUT/DA $\leq$ DB
FOR	$\equiv$	Tape must be in forward direction
CI	$\equiv$	Comparison is inhibited
$\overline{CI}$	$\equiv$	Comparison is not inhibited
REV	$\equiv$	Tape must be in reverse direction
e	$\equiv$	UUT/DA = DB
AF	$\equiv$	Address follows command
AOK	$\equiv$	Address OK
ANT	$\equiv$	Address not there

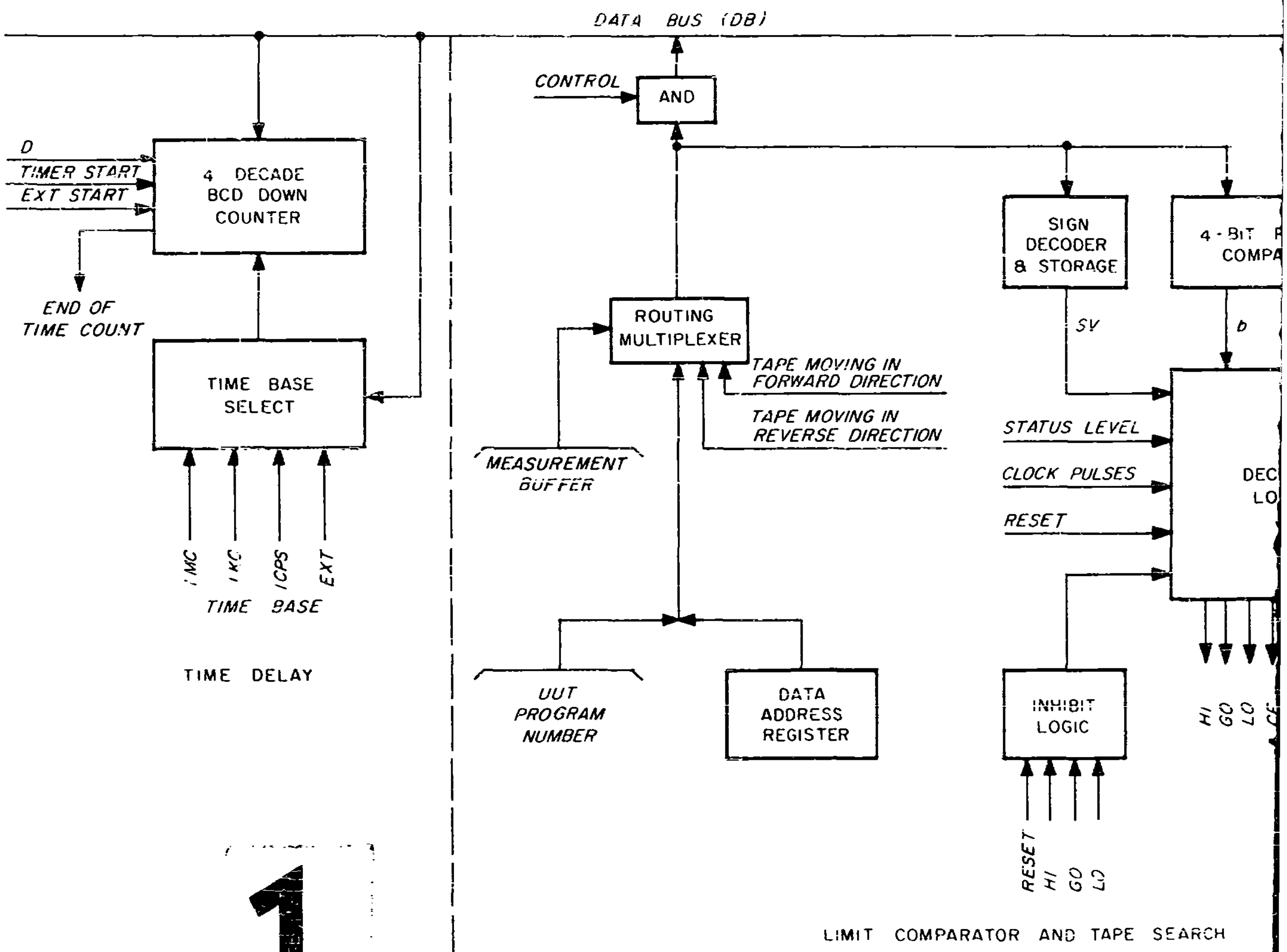

Figure E-[illegible]. Comparator time delay unit block diagram

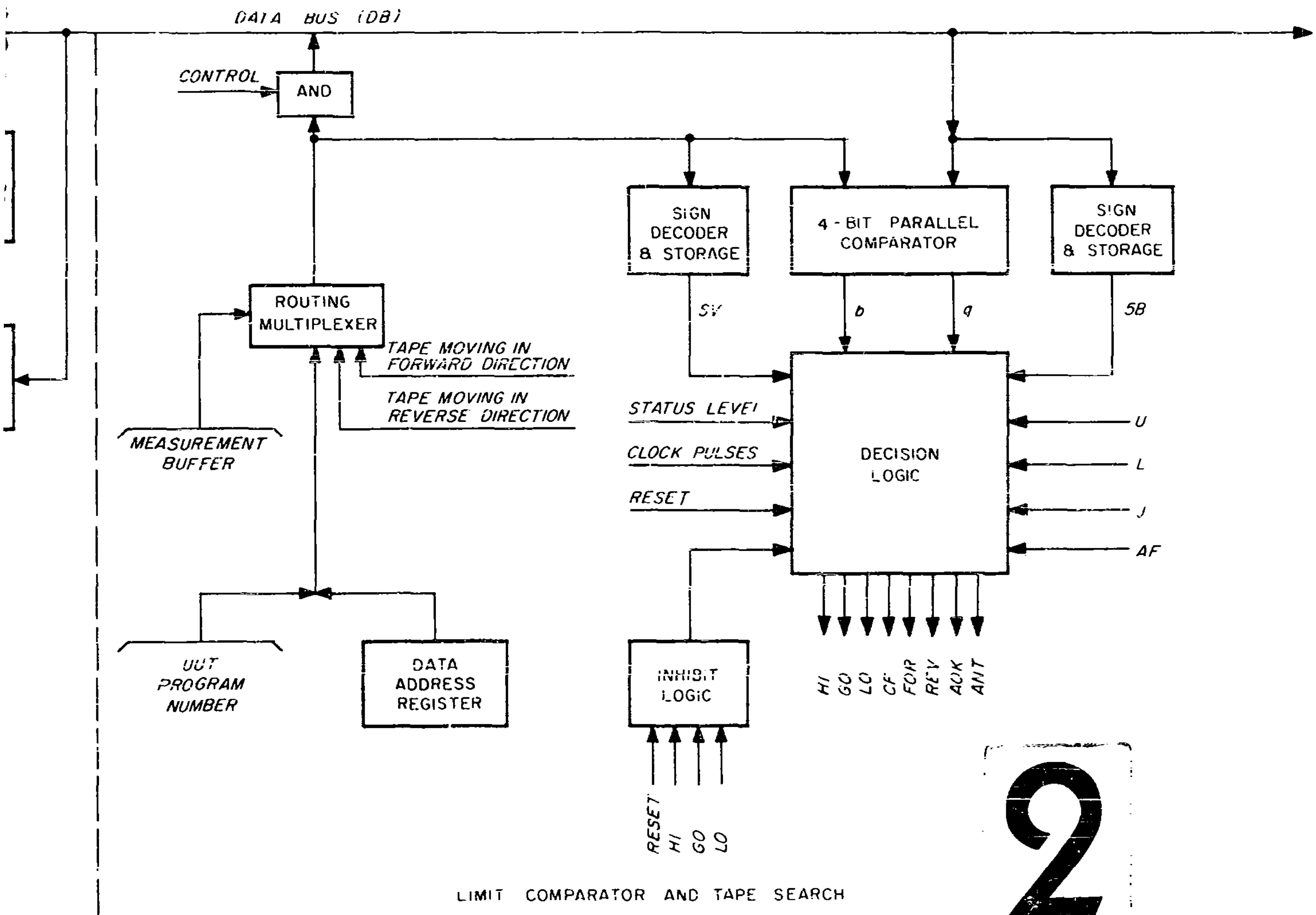

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Figure E-2. Comparator time delay and block diagram

APPENDIX F

DIGITAL MULTIMETER INPUT

F.1 GENERAL

The input circuit of the digital multimeter consists of two solid-state choppers driven 180° out of phase. The switching drive is supplied by a 100-Kc square wave transformer coupled to the base-collector diodes. Two identical transformers are used to accomplish the coupling. The two transformers prevent loading of the square wave source and aid in impedance matching and spike reduction in the output.

F.2 FUNCTIONAL DESCRIPTION

Figure F-1 is a schematic diagram of the input circuit. Phasing of the transformers is such that during the first half cycle of the square wave the base-collector junction of Q1 is forward biased with Q2 reverse biased and the unknown level is transferred to the output. The next half cycle of the drive signal forward biases the base-collector junction of Q2 and reverse biases Q1 and causes the dacon output to be impressed on the output. Any difference in the two levels appears at the output and alters the dacon output to bring it closer to the unknown level. When the dacon output is adjusted to within one millivolt of the unknown level, the square-wave drive to the transformer is inhibited and the dacon output is read out as a BCD number.

As a result of directly coupling the two choppers and alternately enabling and inhibiting them, voltage comparison is rapidly and accurately accomplished. Output spikes, due to capacitive coupling in the transformers and differences in transistor characteristics, can be held to 500 microvolts and do not interfere with circuit operation.

The output of this circuit is coupled through a small capacitor to a high (greater than one megohm) input impedance amplifier. This prevents loading of the

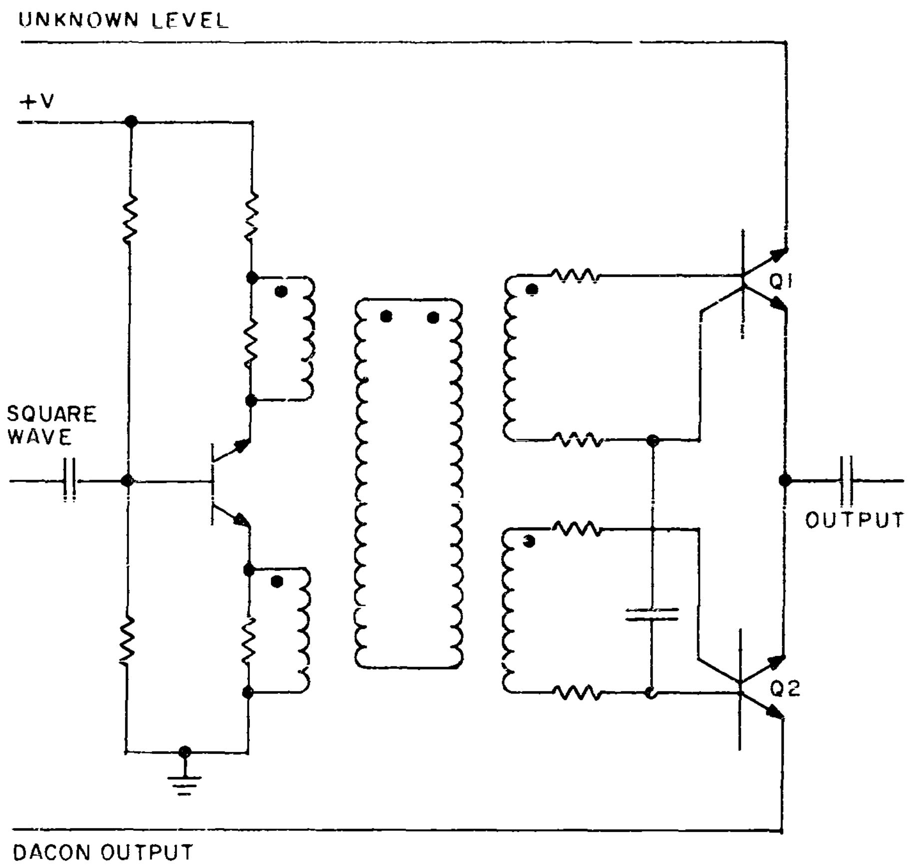


Figure F-1. Digital multimeter input circuit, schematic diagram

source voltages and limits current flow through the choppers, thus reducing offset across the chopper.

APPENDIX G

DACON CURRENT SWITCHING REQUIREMENTS

In the Digital Multimeter the sum of the errors from the four decades (thousands, hundreds, tens, units) cannot exceed 1 millivolt in order to meet the required accuracy of 0.01 percent at 10 volts. See Figure G-1. Assume each of the four identical decades contributes one-fourth of the total error; then

$$
\begin{array}{lll}
\text{Decade } 1 \text{ (thousands)} & = V_1 & = 0.25 \text{ mv} \\
\phantom{\text{Decade }} 2 & = V_2 & = 0.25 \text{ mv} \\
\phantom{\text{Decade }} 3 & = V_3 & = 0.25 \text{ mv} \\
\phantom{\text{Decade }} 4 & = V_4 & = 0.25 \text{ mv}
\end{array}
$$

Since V_2 through V_4 are obtained from the dividers shown, the divider inputs can be as high as

$$V_2' = 2.5 \text{ mv}$$
$$V_3' = 25 \text{ mv}$$
$$V_4' = 250 \text{ mv}$$

Referred to a normalized 10-volt level, these values correspond to

$$V_2' = 0.025\%$$
$$V_3' = 0.25\%$$
$$V_4' = 2.5\%$$

From a circuit development point of view, it is relatively easy to hold V_4' to 1 percent, V_3' to 0.1 percent, and V_2' to 0.01 percent. If the contribution from

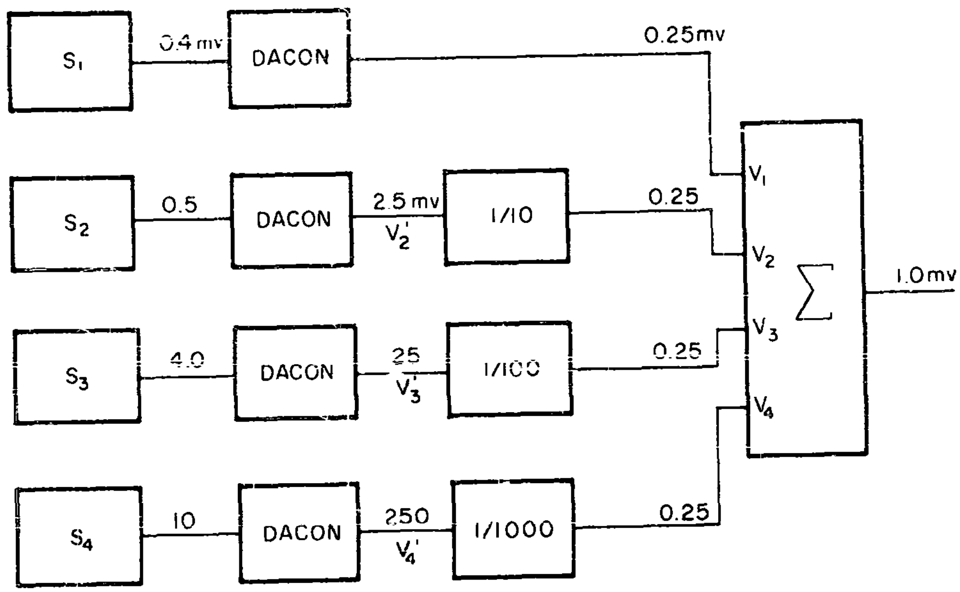


Figure G-1. Digital multimeter dacon current switching - block diagram

V_i is tightened slightly to 0.002 percent, then the actual errors at the dacon outputs and weighted values at the divider outputs will be:

		Error (Percent)	Actual Error (Millivolts)	Weighted Value (Millivolts)
Decade	1	0.002	0.2	0.20
	2	0.01	1.0	0.10
	3	0.10	10.0	0.10
	4	1.00	100.0	0.10
			Total	0.50

The above discussion permits the dacons and dividers to contribute 0.5 mv error; therefore, 0.5 mv can be budgeted for the switches if the total error is not to exceed 1.0 mv. A reasonable distribution of errors due to the switches is

	Actual Error Permitted (Millivolts)	Weighted Error-Following Dividers (Millivolts)
S_1	0.4	0.4
S_2	0.5	0.05
S_3	4.0	0.04
S_4	10.0	0.01
	Total	0.50

Transistor data indicates that the best single, selected transistor may have V_{ec} characteristics of five to ten millivolts. Therefore only Decade 4 could be a single-transistor-type switch. This condition led to a dacon-switch for Decades 1, 2 and 3 are shown schematically in Figure G-2. The circuit is essentially a 3PDT switch composed of difference and feedback amplifiers arranged to minimize the effects of transistor parameter variations. To maintain standardization throughout the Multimeter, Decade 4 will use the same circuitry as the other decades. The circuit of Figure G-2 provides

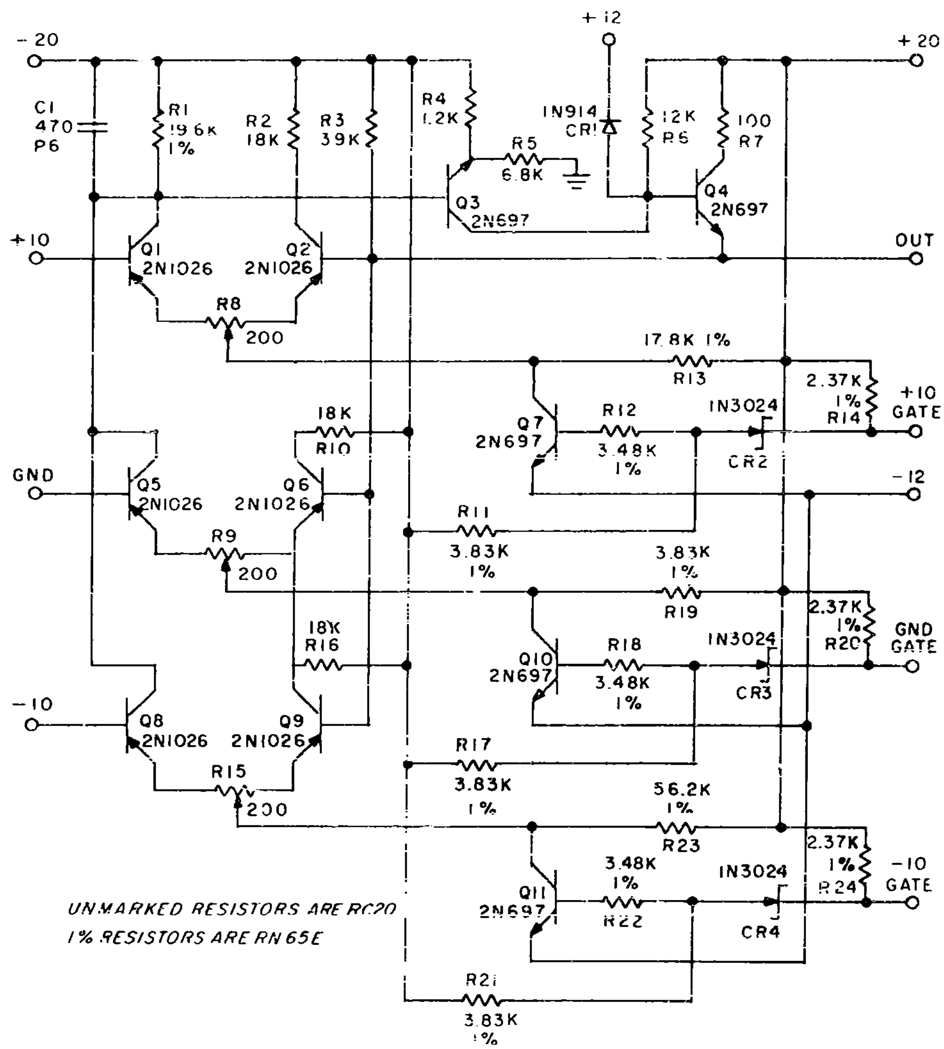


Figure G-2. 10^3 decade dacon switch

one-fourth of the requirements per decade; there are four per decade, or a total of 16 for the Multimeter.

APPENDIX H

POSITIVE REGULATOR CALCULATIONS

A set of calculations for loop gains, output resistance, AC stability, and breakpoints is presented in Figure H-1. These calculations, although specifically for the +12 volt regulator, are typical of the procedure followed for all the other positive regulators. The calculations made are as follows:

<u>Sheets 1 and 2</u>

Calculations for maximum and minimum open loop gain

<u>Sheet 3</u>

Calculations of maximum and minimum loop gain with use of feedback ratio, and calculation of DC output resistance

<u>Sheet 4</u>

Calculation of network for AC stability

<u>Sheet 5</u>

Calculation for determining breakpoints of tantalum capacitor

<u>Sheet 6</u>

A Bode plot of gain versus frequency indicates that the circuit is stable for maximum and minimum gains

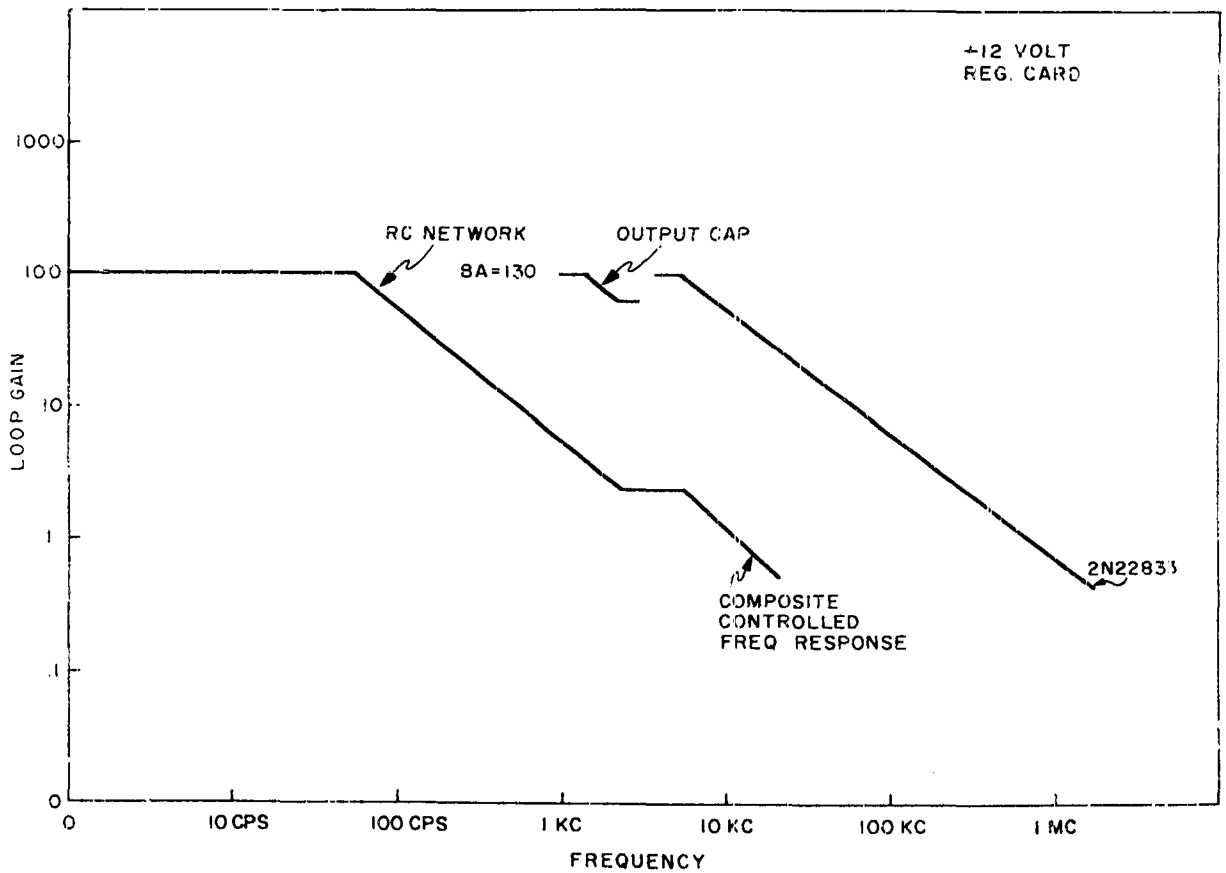


Figure H-1. Typical calculation for gain stability

Loop Gain

Gain $Q_1 \cong$ Gain Q_2

$$A_V = \frac{BRL}{2\,[Rb + rb + (\beta + 1)(re + RE)]}$$

$$R_L = R_{3,7} \,||\, (\beta + 1)(R_{9,10})$$

$$120\,(.47) = 56K$$

$$R_L = 5.62K \,||\, 56K = \frac{5.6\,(56)}{62} \cong 5K$$

$$Rb + rb + (\beta + 1)(re + RE)$$

$$.75 + 1.0 + 120\,(.025 + .1)$$

$$1.75 + 120\,(.125)$$

$$1.75 + 15 \approx 16.8K$$

$$A_V = \frac{120\,(5)}{2\,(16.8)} = 18$$

Gain $Q_3 \approx Q_4$

$$A_V = \frac{120\,(12.1)}{2\{1 + 120\,(.06 + .47)\}} = \frac{120\,(12.1)}{2\,\{65\}} = 11$$

$$A_V \text{ TOT} = 2 \times 18 \times 11 \cong 400 \text{ max gain}$$

Parameter Assumptions

2N1893

$$re = \frac{25 \text{ mw}}{Ic} = 25\,\Omega$$

$rb = 1K$

$\beta = 120$

$$Rb\,Q_2 = 1.5K \,||\, 1.5K$$

$$= 750\,\Omega$$

Looking back into
Voltage adjusting pot

Figure H-1 (sheet 1 of 5)
Typical Calculation for Gain and Stability (Open Loop Gain)

Minimum Gain $\qquad$ Gain $Q_1 \cong$ Gain Q_2

For minimum gain use $\beta \cong 40$

$$A_V = \frac{BRL}{2\,[Rb + rb + (\beta + 1)(re + RE)]}$$

$$R_L = 5.6K \parallel 40\,(.47) \cong 20K$$

$$R_L = \frac{5.6\,(20)}{25.6} = 4.4K$$

$$Rb + rb + \beta + 1\,(re + RE)$$

$$.75 + 1.0 + 41\,[.125]$$

$$1.75 + 5.1 = 6.8$$

$$A_V = \frac{40\,[4.4]}{2 \times 6.8} = 13$$

Gain $Q_3 \cong Q_4$

$$A_V = \frac{40\,(12.1)}{2\,[1 + 40\,(.06 + .47)]} \cong 11.5$$

$$A_V = \frac{40\,(12.1)}{2\,(21)} = 11.5$$

$$A_V\ TOT = 2 \times 13 \times 11.5 \cong 300 \text{ min gain}$$

Nominal Gain = 350

$A_V\ TOT = 2 \times 13 \times 11.5 \cong 300$ min gain

$A_V = \frac{40\,(12.1)}{2\,(21)} = 11.5$

Nominal Gain = 350

Figure H-1 (sheet 2 of 5)
Typical Calculation for Gain and Stability
(Open Loop Gain, Continued)

Q_5, Q_6, and Q_7 are all emitter followers. Overall gain estimate for these three stages is about 0.75 to the output terminals.

$$350\,(.75) = 260$$

Feedback Ratio $= \beta = 1/2$

$$\text{Loop Gain} = \beta A = 1/2\,(260) = 130$$

Output Resistance

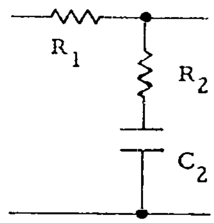
$$R_O \text{ (open loop)} = 0.2\,\Omega$$

$$R_O \text{ (closed loop)} = \frac{R_O \text{ open loop}}{1 + \beta A}$$

$$= \frac{0.2}{130} = .0015 \text{ ohms}$$

Figure H-1 (sheet 3 of 5)
Typical Calculation for Gain and Stability
(Loop Gain Using Feedback Ratio Output Resistance)

Break-Point



$$T_1 \cong (R_1 + R_2)\, C_2$$

$$T_2 = R_2\, C_2$$

$$T = \frac{1}{2\pi f} \qquad f = \frac{.159}{T}$$

1st Break at 50 cps

$$T_1 = \frac{.159}{50} = 3.18 \text{ ms}$$

Level off at 1.5 kc

$$T_2 = \frac{.159}{1.5 \text{ kc}} = .108 \ \mu\text{sec}$$

$R_1 = 12K$

$$T_1 = 3.18 \times 10^{-3} = (12K + R_2)\, C_2$$

$$T_2 = .108 \times 10^{-3} = R_2\, C_2 \qquad R_2 = \frac{.108 \times 10^{-3}}{C_2}$$

$$3.18 \times 10^{-3} = 12 \times 10^{3}\, C_2 + .108 \times 10^{-3}$$

$$C_2 = \frac{3.18 \times 10^{-3} - .108 \times 10^{-3}}{12 \times 10^{3}}$$

$$C_2 = \frac{3.07 \times 10^{-3}}{12 \times 10^{3}} = \underline{.25\ \mu\text{fd}}$$

$$R_2 = \frac{.108 \times 10^{-3}}{.25 \times 10^{-6}} = \frac{10.8 \times 10^{-5}}{2.5 \times 10^{-7}} = \frac{10.8 \times 10^{2}}{2.5} = 430\,\Omega$$

choose .22 μfd and 470 Ω

Figure H-1 (sheet 4 of 5)
Typical Calculation for Gain and Stability (AC Stability Considerations)

Break Point - Output Capacitor

Typical ESR output capacitor = 1 ohm at 1kc

Output R_O = .2 ohms

$$f = \frac{1}{2\pi RC} = \frac{.159}{(1 + .2)\ 110 \times 10^{-6}} = 1.3\ \text{kc}$$

ESR drops to about 0.8 Ω at 2kc

$$f = \frac{1}{2\pi RC} \quad \frac{.159}{.8 \times 110 \times 10^{-6}} = 2\text{kc} \quad \text{it levels off}$$

Figure H-1 (sheet 5 of 5)
Typical Calculation for Gain and Stability

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1. Design of standard millimodules and millimodule boards
2. Rack and chassis mechanical drawings
3. Shelter-rack interface
4. Layout and design display control equipment
5. Vendor selection for peripheral equipment

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UNCLASSIFIED

1. Design of standard millimodules and millimodule boards
2. Rack and chassis mechanical drawings
3. Shelter-rack interface
4. Layout and design display control equipment
5. Vendor selection for peripheral equipment

I. Army Missile Command, Redstone Arsenal

II. Contract DA-36-034-ORD-3650 Z

UNCLASSIFIED

Radio Corporation of America, Camden, N.J., Burlington, Mass.

FOURTH QUARTERLY INTERIM TECHNICAL REPORT
15 May 1963, 375 pp. incl illus, tables (Report No. CR-63-547-37) (Contract DA-36-034-ORD-3650 Z).

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